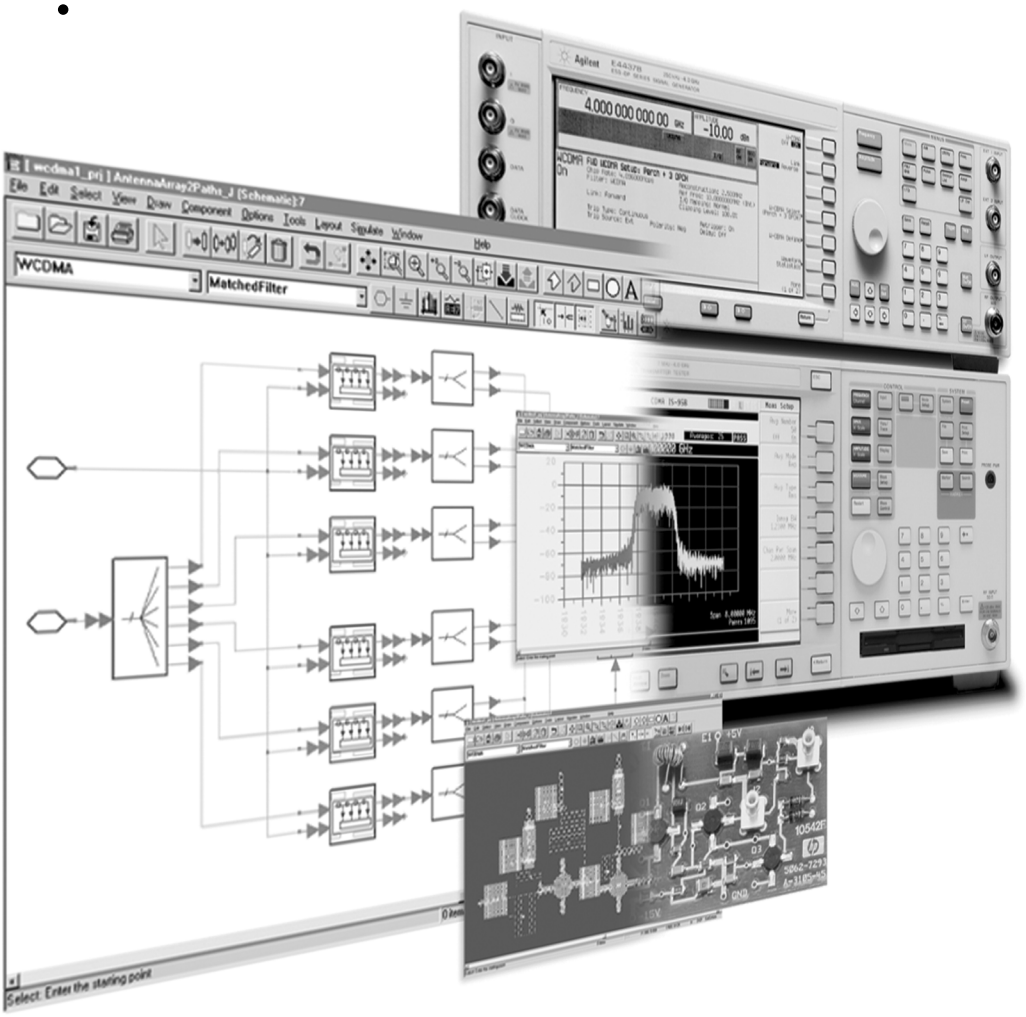
Connected Simulation and Test Solutions Using the Advanced Design System

Application Note Number 1394



Agilent Technologies

Contents

Appendixes

Introduction: Why make Design Verification Easier?

Designing and verifying designs to today's complex signal formats can present some interesting challenges. Designs can be verified in simulation and they can later be verified after all of the hardware returns from fabrication -- but an intermediate level of verification early in this design/fabrication cycle can be difficult to achieve because it may require all, or most of, the prototype hardware. Fabrication cycle time often results in inefficiencies while designers wait for hardware before performing verification testing. Add a couple of design iterations to this, and design time really adds up.

Some typical problems are:

- The hardware returns from fabrication and the system does not meet the original design specifications. Isn't there a way to evaluate system level performance even earlier with partial hardware, to help minimize risk and costs?

- I use my design tool in the simulation/design phase, then transition to test equipment for the testing phase. How can I get more consistency between my design and test solutions for better design predictability? How can I transition back into my design tool for design modifications if the hardware is not performing correctly on the test bench?

- I'd like to begin Bit Error Rate testing of my RF hardware, but it requires baseband functionality, which isn't available yet. How can RF testing begin before the baseband sections are done?

- I can test components with "ideal" signals, but how can I evaluate my DUT (Device Under Test) with custom test signals that reflect how the component will be used in the system?

- How can I evaluate re-using hardware with a new signal format or new design modeled in simulation before building all of the hardware? How do I test hardware if the new signal format isn't available as a test solution?

With connected simulation and test solutions from Agilent Technologies, the designer's testbench consists not only of test equipment, but also includes the Advanced Design System (ADS) for design and simulation of systems and circuits. These connected solutions let designers quickly perform simulations to evaluate design trade-offs and what-ifs, and then turn the simulated signal into a real RF test signal on the testbench for hardware test. Conversely, designers can take the measured output signal from the Device Under Test (DUT) and bring it into ADS for additional analysis in the simulation environment.

System designers can benefit from connected solutions because it can help:

- Evaluate system-level performance with partial RF hardware, using simulation to model missing hardware.
- Evaluate RF performance (such as BER), using simulation to model missing baseband functionality
- Evaluate system performance more continuously throughout the design/fabrication cycle to help reduce risk and costs.
- Evaluate system performance on the testbench with simulated impairments such as fading or multi-path.

Component designers benefit from connected solutions because they can use realistic signals for testing that reflect the environment in which the component will be used. Applications include:

- Testing/demonstrating a component DUT – Modeling a transmitter/receiver chain in simulation to show how it would perform in a system.
- Testing/demonstrating a component with various signal formats modeled in simulation – possibly signal formats which are not currently available as test solutions.
- Evaluating performance limits of a DUT – how impaired can the input signal be and still meet specifications?

Figure 1 shows the complete signal path flow that is possible with an Agilent connected solution. The signal originates in the simulation design tool and then is created on the test-bench for use as a real-world test stimulus for a DUT. After a signal is passed through the DUT, it might be input into a signal analyzer, recorded, and then brought back into the simulation design tool to use as a simulation signal source for further simulation and analysis.

This application note discusses the connected signal source capability between ADS and the ESG arbitrary waveform generator from Agilent Technologies, and the connected signal analysis capability between ADS and signal analyzers using the 89600 software simulation source and measurement from Agilent Technologies. Case studies and examples illustrate how to apply connected solutions to specific applications.

Although, for consistency, the case studies in this application note revolve around a W-CDMA signal format, connected solutions are a powerful general-purpose capability, which can be used for many other applications and signal formats. Appendixes to this application note illustrate connected solution setups for other signal formats such as WLAN 802.11a, EDGE, and 1xEV-DO.

This application note touches on only a small sample of the potential applications for these connected solutions. Designers will discover their own applications as these connectivity solutions become more widely understood.

This application note assumes that the reader has basic familiarity with digital communications concepts, with Advanced Design System, and with Agilent signal sources and analyzers. Appendix H contains some useful references, as well as relevant training courses that are available for Agilent products. Please contact your local Agilent Technologies representative for additional information. To find your local representative, visit **www.agilent.com/find/assist.**

Downloadable projects

The ADS projects described in this application note may be downloaded from **http://eesof.tm.agilent.com/applications/** Use them as a basis for your own unique and specific applications.

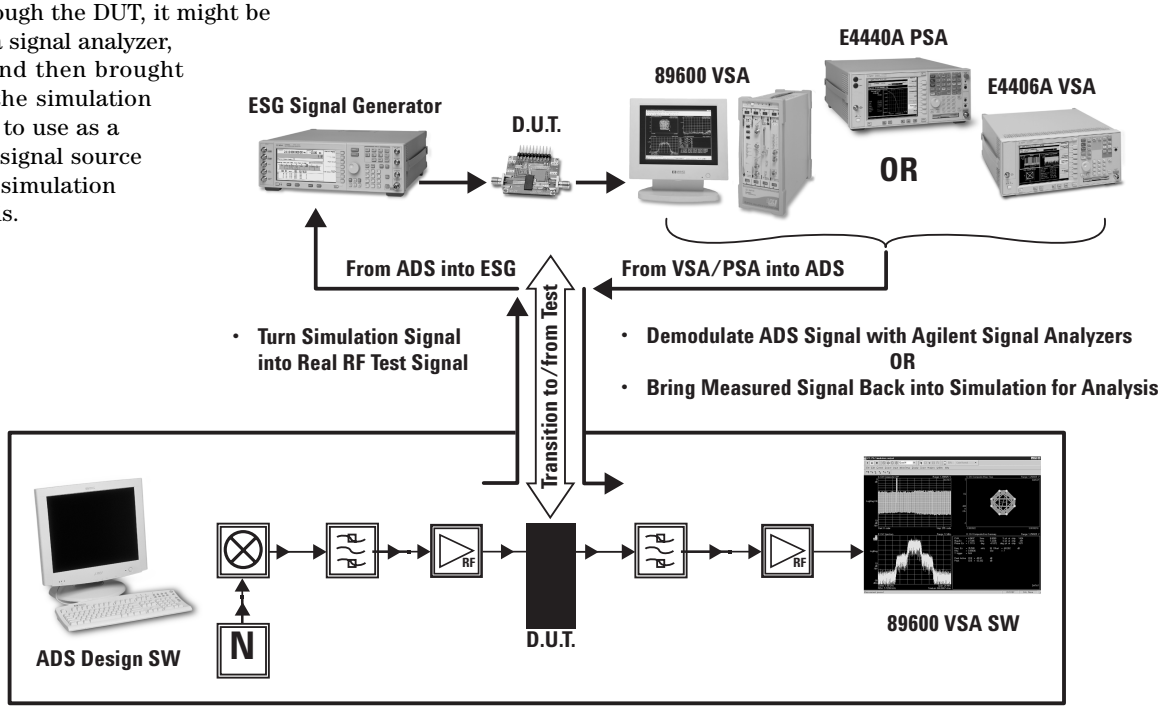


Figure 1. Signal path flow for connected solutions.

Using Connected Signal Source Solutions to Model a Signal and Turn it into a Real RF Test Signal on the Testbench

This section discusses combining the flexibility of simulation with signal source test capabilities to create custom, real-world test signals on the testbench.

This capability involves modeling a signal or design in ADS and using the ADS-ESG sink to download the waveform into the ESG's arbitrary waveform generator (option UND for E443XB ESG, and option 001 or 002 for E4438C ESG). This section discusses the fundamentals of setting up the ADS-ESG sink to create real-world test signals.

Some applications for the ADS-ESG sink are described in the example case studies that follow in this application note.

ADS-ESG Connected Signal Source Solutions

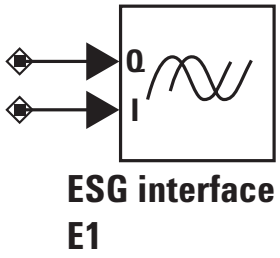


Figure 2. ADS-ESG Sink Element.

Figure 2 shows ADS-ESG sink element in ADS. The ADS-ESG Sink collects simulated data and downloads it to the ESG signal generator when the simulation is complete. The ESG sink is placed into the DSP schematic window, along with the design being modeled, and the I and Q are connected to the point in the design where the desired signal is to be created.

Why I and Q Inputs? In digital communications, modulation formats are often expressed in terms of I and Q. This is a rectangular representation of the polar diagram. On a polar diagram, the I axis lies on the zero degree phase reference, and the Q axis is rotated by 90 degrees. The signal's vector projection onto the I axis is its "I" component and the projection onto the Q axis is its "Q" component, as shown in figure 3.

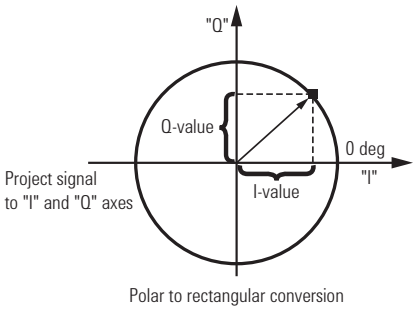


Figure 3. I-Q Format.

Note: "ESG" is used throughout the application note to refer to the E443XB ESG signal generators. The E443XB ESG was used for all of the case studies presented in this section of the application note, as well as the 1xEV-DO and EDGE appendixes. The E4438C ESG also could have been used for these case studies. The E4438C ESG was used in the connected solution BER case study as well as the WLAN 802.11a example in Appendix C.

Note: The magnitude of the signal can be expressed as sqrt (I^2 + Q^2) and the phase of the signal can be expressed as arctan (Q/I). Thus, the magnitude and phase of an arbitrary signal can be described in terms of its I component and its Q component. If the arbitrary signal's magnitude and phase is changing as a function of time, then its magnitude as a function of time can be described as sqrt (I(t)^2+Q(t)^2) and its phase as a function of time can be described as arctan (Q(t)/I(t)), where I(t) and Q(t) are the I and Q waveforms as a function of time, respectively. The ADS sink element accepts I and Q samples as defined by its Start and Stop parameters and download these samples into the ESG signal generator's arbitrary waveform generator to create a test signal with arbitrary amplitude and phase as a function of time.

The ADS-E443XB ESG Sink and its Parameters

Figure 4 shows a picture of the ADS-E443XB ESG sink with its parameters displayed with their default values. This section discusses each parameter and its corresponding function. Note that this ADS-ESG sink is intended for use with the Agilent E443XB series ESG signal generators and has a different set of parameters than the ADS sink for the E4438C ESG signal generator discussed in the next section.

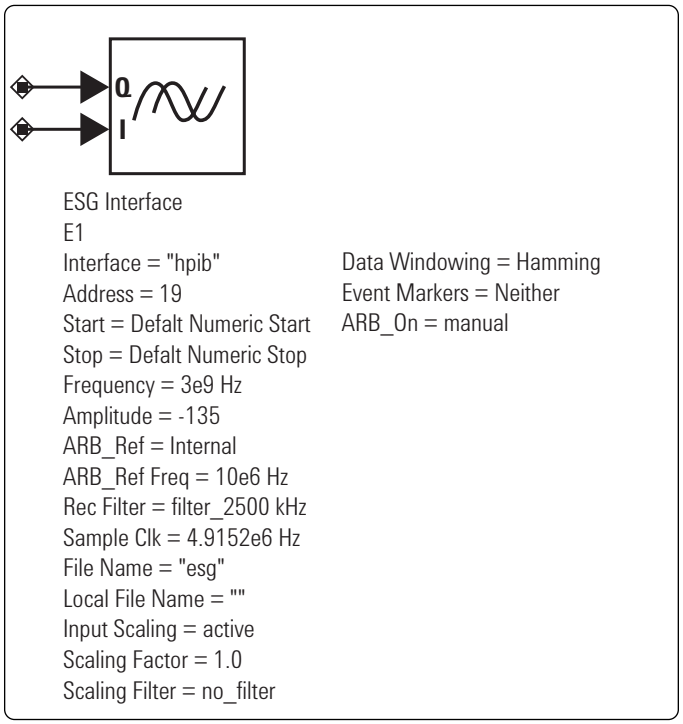


Figure 4. ADS-E443XB ESG Sink Element and Its Parameters.

1. "Interface" Parameter. This required parameter defines whether a General Purpose Interface Bus (GPIB) or a Local Area Network/Internet Protocol (LAN/IP) Gateway is being used to communicate with the instrument. This is discussed in more detail in the next section.

2. "Address" Parameter. This required parameter specifies the address of the ESG. If this address is not known, check it by pressing "Utility," followed by "GPIB/RS-232" on the ESG signal generator front panel. The GPIB address is shown on the top of the display and can be entered for the "Address" parameter in the ADS-ESG sink element. This address parameter is required when using either the GPIB interface card or the LAN/GPIB gateway.

3. "Start" and "Stop" Parameters. These required parameters define when to start and stop data collection for the ESG sink. The I and Q inputs for the ESG sink are floating point, so a TimedToCx element followed by a CxToRect element can convert the timed signal into a floating point rectangular (I & Q) representation if a timed signal is being simulated in the ADS schematic. The TimedToCx converts a timed signal to a complex I & Q representation on a single output pin, while the CxToRect splits the I and Q components into separate pins.

   The number of samples collected (Stop-Start+1) must be in the range of 16 to 1,048,576 and should be an even number of samples. The last sample is discarded if Stop-Start +1 is odd.

   Carefully consider the Start and Stop parameters for the ESG sink. The ESG sink downloads the I and Q samples from ADS to the ESG's arbitrary waveform generator upon completion of the ADS simulation. These samples are then repeated continuously every 1,048,576 samples to create a periodic signal, thus any signal shorter than 1,048,576 samples in duration looks like a "zero-padded" signal as it repeats in the ESG signal generator.

Note: The ESG4438C Sink may be used instead with the E4438C ESG signal generator if more samples need to be downloaded for a given application. The ESG4438CSink is discussed in the next section of this application note.

It is useful to select a "Start" value, which accounts for any delays in the data being input into the ESG sink. For example, if there is a 100-tap Finite Impulse Response (FIR) filter at the input of the ESG sink, then no signal data will come out of the FIR until 50 samples (one-half of the filter length). The "Start" parameter could then be set to 50, so that it will not gather any data until there is valid signal data at its input pins.

The "Stop" parameter can then be selected to download between 16 and 1,048,576 samples. If a signal format with a frame structure cdma2000, 1xEV, WLAN, and so on...) is being simulated, then the "Stop" parameter can be selected such that an integer number of frames is downloaded into the ESG's arbitrary waveform generator. For example, 3GPP W-CDMA has a frame length of 10 ms and a chip rate of 3.84 MCps. Thus, 1 frame of data contains 3.84e6 chips per second x 10e-3 seconds/frame = 38,400 chips per frame. At four samples per chip, one frame of data would contain 38,400 chips x 4 samples/chip = 153,600 samples/frame of data. Thus, approximately six integer frames of data can be downloaded from ADS into the ESG signal generator's arbitrary waveform generator to meet the 1,048,576 sample limit (153,600 samples/ frame x 6 frames = 921,600 samples). The E4438C ESG can be used instead if more samples are required.

4. "Frequency" and "Amplitude" parameters. These are the signal frequency and amplitude to be set on the ESG signal generator. These can also be altered on the front panel of the ESG after downloading the ADS data by pressing "Local" then either "Frequency" or "Amplitude" on the front panel.

5. "ARB_Ref" parameter. Specifies an internal or external reference for the ESG clock generator. If set to External, the "ARB_RefFreq" parameter sets the frequency of this clock. Acceptable values range from 250 kHz to 20 MHz. Leaving "ARB_Ref" set to its default "Internal" setting and "ARB_RefFreq set to its default "10e6Hz" setting should be acceptable for most applications.

6. "ARB_RefFreq" parameter. Specifies the reference frequency of the external reference signal if "ARB_Ref" is set to "External"

7. "RecFilter" parameter. Specifies the bandwidth (cutoff frequency) of the lowpass reconstruction filter in the ESG at its Digital-To-Analog (DAC) output. The selection choices are through (none), filter_250kHz, filter_2500kHz, filter_8MHz, and standard.

   This parameter should be selected while considering the bandwidth of the signal to minimize potential anti-aliasing products. In general, a filter bandwidth should be selected which is wider than the signal bandwidth to avoid creating inter-symbol interference. Applying a filter may improve the signal quality by reducing the amount of noise or anti-aliasing effects if performing in-channel measurements such as Error Vector Magnitude (EVM). Setting the "RecFilter" parameter to "through," however, may be desirable if performing wideband measurements such as Adjacent Channel Leakage Ratio (ACLR) since the RecFilter may attenuate the out-of-band signal energy beyond its cutoff frequency.

Note: Setting "ARB_Ref" to "external" without having an external reference connected can produce an unexpected spectrum (typically much narrower than expected).

8. “SampleClk” parameter. This parameter sets the sample clock rate for the DAC output in the ESG signal generator. Acceptable values range from 1 Hz to 40 MHz. It is convenient to set this parameter to the sampling frequency used in the ADS simulation. For example, the “SampleClk” could be set to 30.72 MHz (3.84 MHz*8) if considering a 3GPP W-CDMA signal with a chipped symbol rate of 3.84 MHz at 8 samples/chip.

9. “FileName” parameter. Sets the name of the waveform inside the ESG’s arbitrary waveform generator that holds the downloaded data. If the “FileName” is empty, the model will not attempt any communication with the instrument. This is useful when the LocalFileName parameter is set (see section for LocalFileName below). The Arb file in the ESG will be overwritten if repeated simulations are performed.

   To view or select the downloaded arbitrary waveform data file on the ESG, select “Local” > “Mode” > “Arb Waveform Generator” > “Dual Arb” > “Select Waveform”. Select the desired waveform and press “Select Waveform”. Press “Mod On/Off” and “RF On/Off” to turn on modulation and RF output power.

10. “LocalFileName” parameter. Sets the name of a local file to which I and Q data are saved. If set to esg, for example, the files esgI.bin and esgQ.bin are saved in the data directory. The esg_arb utility can then download these files outside of ADS. If LocalFileName is empty, then no files are written. Local files are saved only when the “SignalFilter” parameter (see below) is set to no_filter.

11. “InputScaling” and “ScalingFactor” parameters. Specify whether to scale the I and Q inputs and what the scaling factor is, if active. If “InputScaling” is set to active, inputs are scaled to ± “ScalingFactor”; if set to inactive, any data with an absolute magnitude larger than 1V is interpreted as 1V.

12. “SignalFilter” parameter. Used to select a suitable filter that will filter data before it is sent to the ESG. For W-CDMA (including 3GPP W-CDMA) signals, this is a root raised-cosine filter; for IS-95 and cdma2000 signal, this is an IS-95 modified filter or an IS-95 modified filter with equalizer. Filter options are for CDMA signals at specified chip rates and include compensation for appropriate ESG reconstruction filters and D/A sin(x)/x roll-off, except as explicitly indicated in Table 1.

Note: The total number of samples supported by the ESG arbitrary waveform generator is 1,048,576 samples. This is the total number of samples of all arbitarary waveform files combined, so there may be less than 1,048,576 samples available if there are other arbitrary waveform files that have been downloaded into the ESG’s arbitrary waveform generator under a different file name(s). To view the downloaded Arb files in the ESG, select select “Local” > “Mode” > “Arb Waveform Generator” > “Dual Arb” > “Select Waveform.” To delete an existing Arb waveform, select “Waveform Segments”> “Delete Segment”. Cycling power on the ESG clears all previously loaded Arb waveform files.

Signal filter option	Signal chip rate (MHz)	Signal samples per symbol	Number of tap coefficients	Rec filter option required	Use with
No_filter	any	any	1	any	
WCDMA_4096 MHz_chip rate	4.096	4	200	2500 kHz	ARIB W-CDMA signals
WCDMA_8192 MHz_chip rate	8.192	4	112	8 MHz	ARIB W-CDMA signals
WCDMA_16384 MHz_chip rate	16.384	2	64	8 MHz	ARIB W-CDMA signals; does not include sin(x)/x compensation for ESG D/A
IS-95_mod_32x8_2500k	1.2288	8	255	2500 kHz	IS-95 or cdma2000 signals
IS-95_mod_EQ_32x8_2500k	1.2288	8	255	2500 kHz	IS-95 or cdma2000 signals
IS-95_mod_24x5_2500k	1.2288	5	120	2500 kHz	IS-95 or cdma2000 signals
IS-95_mod_EQ_24x5_2500k	1.2288	5	120	2500 kHz	IS-95 or cdma2000 signals
W-CDMA_3GPP_56x4_2500k	3.84	4	224	2500 kHz	3GPP W-CDMA signals
W-CDMA_3GPP_64x4_2500k_H99	3.84	4	256	2500 kHz	3GPP W-CDMA signals and when ESG has Option H99 for low ACPR engaged

Table 1. Signal Filters Available in ADS-E443XB ESG Sink.

The "SignalFilter" parameter should be set to "No_Filter" if the simulation contains a transmit filter in the RF modulator. For example, the ADS 3GPP design library includes a root raised-cosine (RRC) filter inside the RF modulator so the "SignalFilter" should be set to "No_Filter" if the RRC filter is simulated. Some of the "SignalFilter" options include compensation, which is not included in the ADS RRC filter. This compensation may result is a slightly better performance, and perhaps a lower residual EVM (for example, the EVM for an "ideal" signal). The ADS RRC filter should not be simulated when selecting a "SignalFilter" on the ADS-ESG sink.

13. "DataWindowing" parameter. Specifies the type of windowing (Hamming, pseudoRectangular, threePtAverage, Hann, Blackman, no_Windowing) to apply to the input data. The Arb data downloaded into the ESG's arbitrary waveform generator is time-limited by the number of samples downloaded. This finite number of samples is repeated continuously, and "DataWindowing" can be useful in addressing discontinuities between the first and last data points, if needed.

14. "EventMarkers" parameter. Specifies which ESG Event markers are enabled: Event1, Event2, Both, or Neither. Event markers are useful for synchronizing other instruments to the ESG. Refer to the Agilent ESG-D Series Options UND and UN5 Signal Generators manual, Chapter 2, for more information.

15. "Arb_On" parameter. If the ARB_On parameter is set to automatic the ESG starts generating the signal immediately after simulation data is downloaded; if set to manual, waveform generation must be turned on at the ESG front panel.

The ADS-4438C ESG Sink and its Parameters

The ESG4438C Sink is specifically designed to download data to the E4438C ESG arbitrary waveform generator. It is not intended to be used with E443XB ESGs. The ESG4438C Sink is available for the Advanced Design System, version ADS 2002 or later, and can be downloaded from: **http://eesof.tm.agilent.com/support/supp200.html.** Click on "Add-On Releases" to login and download the Instruments Library.

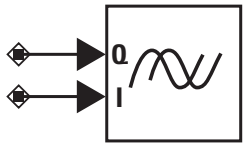
Setting up the ADS-E4438C ESG Sink requires running IO Config. Refer to "Appendix E: Configuring the ESG4438C Sink" for more details.

Figure 5 shows a picture of the ADS-E4438C ESG Sink with its parameters displayed with their default values. Many of the parameters are similar to the ADS-E443XB ESG Sink discussed in the previous section, so only additional parameters and differences for this ADS-E443XB ESG Sink are discussed in this section. Note that this sink is offered only on PC platforms.

1. "Interface" Parameter. The ADS-4438C ESG Sink has a slightly different interface usage than the E443XB ESG Sink. Specifically, the IP address is not directly specified when a LAN/IP Gateway to interface to the E4438C ESG.Instead, the IP address is associated with the GPIB address of the E4438C ESG and the GPIB address is instead used for the "Address" parameter. The "GPIB VISA LAN Client (for example, E2050)" should be configured if using a LAN/IP Gateway to interface to the E4438C ESG. See "Appendix E: Configuring the ADS-4438C ESG Sink" for more details on how to configure the VISA LAN Client.

2. "InterfaceSelector" Parameter. Specifies the interface number of the GPIB or TCPIP IO configuration. This interface number is discussed in "Appendix F, Troubleshooting ADS-ESG Sink issues."

3. "Stop" Parameter. The E4438C ESG allows a larger number of samples to be downloaded into its arbitrary waveform generator (Arb) than the E443XB ESG. Option 002 allows up to 32M samples to be downloaded into the Arb. Option 001 allows up to 8M samples to be downloaded into the Arb.



E1

Interface = "hpib"	ARB On = Yes
Address = 19	RF Pow On = Yes

Interface Selector - 0
Start = Defalt Numeric Start
Stop = Defalt Numeric Stop
Frequency = 3e9 Hz
Amplitude = -135
ARB Ref = Internal
ARB Ref Freq = 10e6 Hz
IQ Mod Filter – through
Sample Clk = 4.9152e6 Hz
File Name = "esg"
Local File Name = ""
Input Scaling = active
Scaling Factor = 1.0

Figure 5. ADS-E4438C ESG Sink Element and its Parameters

4. "IQModFilter" Parameter, This is similar to the "RecFilter" parameter previously discussed for the E443XB ESG Sink. Selections include Through, 2100 kHz, and 40 MHz. The E4438C has a sample rate of 100 MHz. This means that even with high data rate formats, the E4438C will oversample enough to create wide separation between sampling images, making unwanted images easy to filter off. Therefore, in many cases, the 40 MHz reconstruction filter should be selected. Since this filter has a high cut-off frequency, the filter attenuation and phase or group delay distortion at its cut-off frequency will not affect either the spectrum or the modulation quality of the signal.

5. "RFPowOn" Parameter. Provides an option for specifying whether to turn the RF power on immediately after downloading the waveform from ADS.

Creating Real-World Test Signals: Example Case Studies with ADS-ESG Connected Signal Source Solutions

This section applies the fundamentals of using the ADS-ESG sink that are discussed in the previous section. The case studies in this section illustrate some of the types of impairments that can be modeled in simulation to create custom real-world test signals on the testbench using connected signal source solutions. All of the case studies presented in this section utilize the E443XB ESG signal generator, but could also utilize the E4438C ESG instead.

- **Case Study 1.** This baseline (reference) example shows how to create a real RF test signal from simulation using the ADS-ESG sink, and demodulate the test signal with the E4440A PSA, E4406A VSA, and 89640A VSA. It shows good baseline performance for connected signal source applications, and it serves as a reference example and starting point for connected source applications.

- **Case Study 2.** This example shows how to create a real RF test signal with amplitude and phase impairments modeled in simulation. The techniques are useful for early testing/verification of RF hardware, representing missing analog/RF hardware in simulation.

- **Case Study 3.** This example shows how to create a real RF test signal with baseband impairments modeled in simulation. The techniques shown here are useful for early testing/verification of RF hardware with baseband effects considered, representing missing baseband and analog/RF hardware in simulation.

Case Study 1:
Baseline Connected Signal Source Example

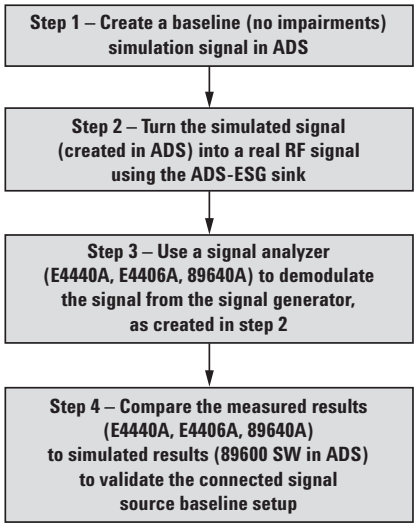


Figure 6. Conceptual Flow for Case Study 1.

This case study follows the conceptual flow diagram shown in figure 6. It shows how to create a signal in simulation and turn it into a real RF test signal on the testbench. The test signal (defined using ADS simulation) is then demodulated with signal analyzers on the testbench, and compared to simulated results for validation. This case study can serve as a reference point for connected signal source applications, since it shows results without simulated impairments.

Step 1. The schematic in figure 7 was created by copying and modifying the WCDMA3G_PA_Test_prj project, which is included with the ADS 3GPP W-CDMA design library (E8875A/AN). The baseline schematic design is shown and consists of an ADS 3GPP W-CDMA uplink source connected to the ADS-ESG sink element.

A "TimedToCx", followed by a "CxToRect" is connected to the ESG sink input. These convert the "timed" signal to floating point I and Q signals for the ESG sink element to process.

The timed sink (labeled T2) connected at the output stores the signal waveform being output by the ADS 3GPP W-CDMA signal source. Examination of the waveform shows that the data coming out of the source begins at approximately 2 µs. This delay is from the baseband root-raised cosine filters in the 3GPP signal source and is considered when setting up the "Start" parameter for the ESG sink. Another useful step is to connect a numeric sink, which displays the waveform as a function of sample (no time step, because the "Start" parameter on the ADS-ESG sink is in terms of a start sample, not a start time.)

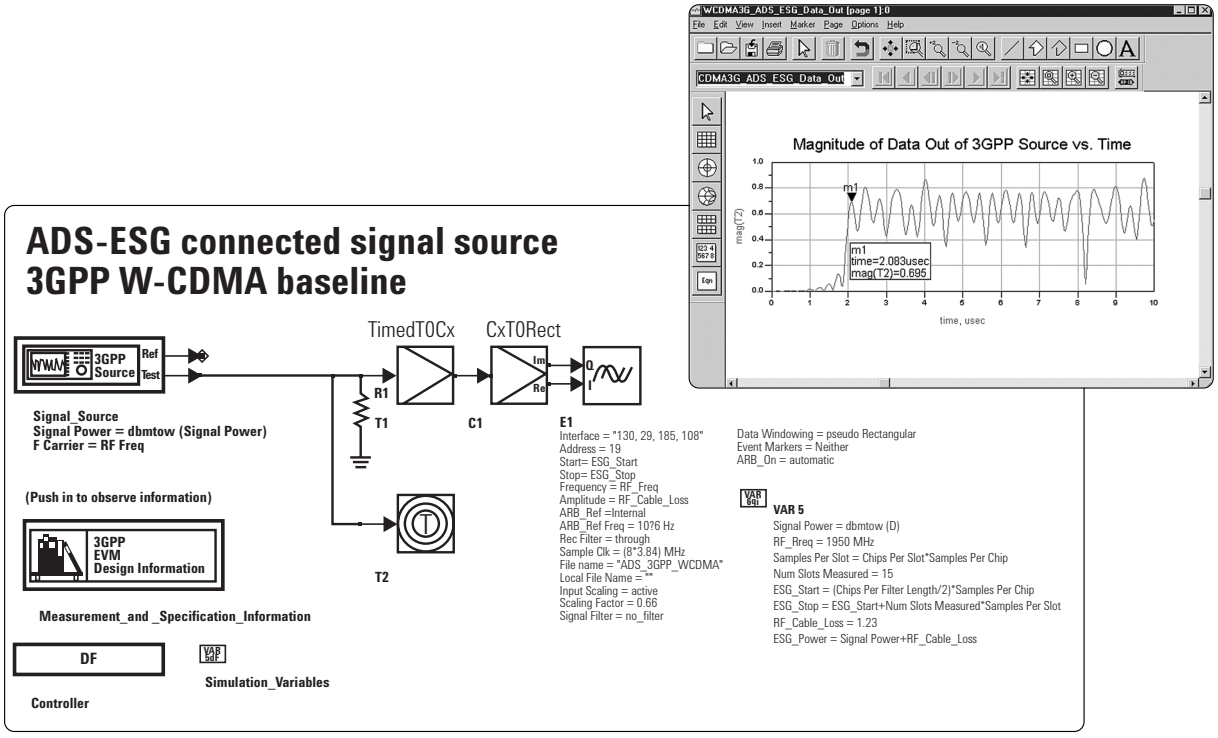


Figure 7. 3GPP W-CDMA Baseline Test Case. Plot of Data Being Input into the ESG (with delay shown) on right.

Step 2. Figure 8 shows a close-up view of the ADS-ESG sink setup and the VAR equations used to calculate some of the parameters. As discussed earlier, the "Start" parameter defines when the ESG sink should start collecting data to download into the ESG signal generator's arbitrary waveform generator. Equations are used to define the parameters for the ESG sink such that it begins collecting data once valid data is available (accounting for the delay observed in figure7), and then collects 15 timeslots of data before downloading the ADS waveform into the ESG's arbitrary waveform generator.

Although not shown in the image, ChipsPerFilterLength is set to 16 symbols and represents the length of the root-raised-cosine filter used in the ADS 3GPP signal source. SamplesPerChip is set to 8, and represents the number of simulation samples per chipped symbol (for example, 8X oversampling of the the 3.84 MHz chip rate, or timestep of 1/(8*3.84MHz)=.032552083 µS). Performing a calculation with these values yields a start sample of ESG_Start=(16/2)*8= 64 samples.

The ESG sink "Stop" parameter is similarly set to the variable "ESG_Stop". This variable calculates the number of samples required to download 15 timeslots, or 1 frame, of 3GPP W-CDMA data into the ESG arb. As discussed earlier, the E443XB ESG arb can hold up to 1,048,576 samples (up to 32 Msamples for the E4438C ESG). The number of samples per timeslot is defined by the variable SamplesPerSlot=ChipsPerSlot*Samples PerChip, which is SamplesPerSlot = 2560*8 = 20,480 Samples/Slot. Thus, 1,048,576 Samples/20,480 Samples/Slot = 51.2 Slots, or 3.41 Frames of data (15 timeslots/frame). For this example, we'll be downloading 15 timeslots of data (1 frame), so the "Stop" parameter is set by the variable "ESG_Stop" which is defined as:

ESG_Stop=ESG_Start+NumSlotsMeasured*SamplesPerSlot, where NumSlotsMeasured is set to 15 timeslots and SamplesPerSlot is set to 20,480 Samples/Slot.

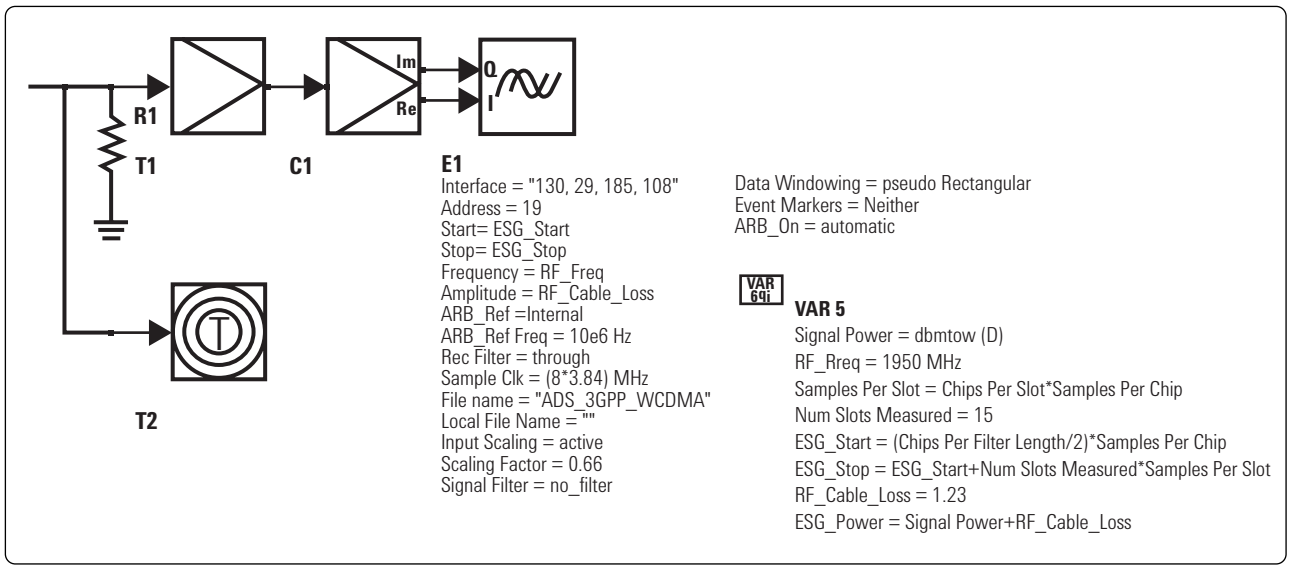


Figure 8. Close-Up view of ADS-ESG Sink setup.

Note: The "Start" parameter on the ESG sink is set to the variable "ESG_Start," which is defined as: ESG_Start=(ChipsPerFilterLength/2)*SamplesPerChip

Note: The ESG sink element defines the "Start" and "Stop" parameters in terms of samples, and not time. The equivalent time can be calculated by multiplying the 64 samples by the timestep, which is the timestamp associated with each sample. Doing so produces an equivalent start time of 64*.032552083 µs= 2.083 µs, which agrees with the time delay observed in figure 7. The ESG_Start parameter is thus set so that it only starts collecting data when valid data is available at its inputs.

Note: The ESG_Stop variable is offset by the ESG_Start variable to account for the delay resulting from the root-raised-cosine filter.

The “Frequency” and “Amplitude” parameters are set to 1950 MHz and +1.23 dBm. The amplitude is set to produce a 0 dBm signal, after compensating for the 1.23 dB cable loss of the RF cable connecting the ESG to the Agilent E4406A Vector Signal Analyzer (VSA).

The “RecFilter” parameter is set to “through”, instead of 250kHz, 2.5 MHz, or 8 MHz. This is set to “through” because Adjacent Channel Leakage Ratio (ACLR) is evaluated at 5 MHz and 10 MHz offset from the 1950 MHz carrier. Applying a “RecFilter” could filter some of the out-of-band energy and alter the ACLR values relative to the out-of-band energy observed in the simulation. The out-of-band suppression is set by the root-raised-cosine (RRC) filter in the ADS 3GPP W-CDMA signal source. Since 8X oversampling is used, any sinx/x amplitude response from the ESG’s Digital-to-Analog (DAC) converter should be fairly negligible over the desired signal bandwidth.

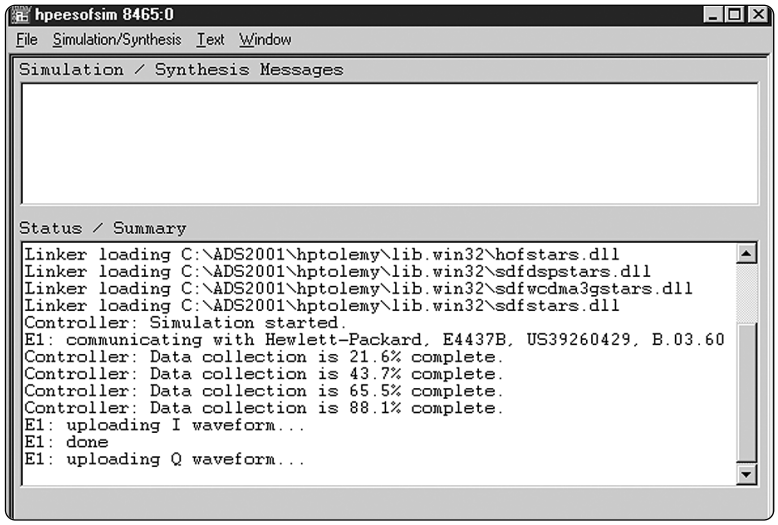


Figure 9. Simulation Status Box Showing I and Q Waveform Download from ADS into the ESG Signal Generator Arb.

The “SampleClk” parameter is set to 8*3.84 MHz, which is the TimeStep sample rate set in the ADS simulation.

“FileName” is set to “ADS_3GPP_WCDMA” which is the name of the Arb filename downloaded into the ESG signal generator’s Arb.

“SignalFilter” is set to “no_filter” because there is a root-raised-cosine filter in the ADS 3GPP W-CDMA signal source providing the transmit baseband filtering. Applying an additional SignalFilter in the ADS-ESG sink would likely result in a distorted signal, since the compliment root-raised-cosine filter is also typically included as a measurement filter in the VSA (resulting in three cascaded root-raised-cosine filters).

The remaining ESG sink parameters are left at their default values. The simulation is performed and the ADS-defined 3GPP W-CDMA signal is then automatically downloaded into the ESG arbitrary waveform generator upon completion of the simulation as shown below in figure 9.

After the I and Q waveforms have been downloaded into the ESG arb, the ADS-defined signal can be activated by pressing the following keys on the ESG front panel:

Local > Mode > Arb Waveform Generator > Dual Arb > Select Waveform> “ARBI:ADS_3GPP_WCDMA”

The **Mod On/Off** and **RF On/Off** on the ESG front panel can then be pressed to turn on the RF output signal, if it isn’t already turned on.

Note: “ADS_3GPP_WCDMA” is the name specified as the “FileName” parameter on the ADS-ESG sink.

Step 3. An Agilent E4440A Performance Spectrum Analyzer (PSA) is connected to the output of the ESG to view the ADS-defined baseline signal as shown in the test setup in Figure 10. The test setup is general, in that either the E4440A PSA, E4406A PSA, or 89640 VSA is used throughout this application note. Baseline results are shown with each of these signal analyzers initially, but a specific signal analyzer is used for each specific application later in the application note.

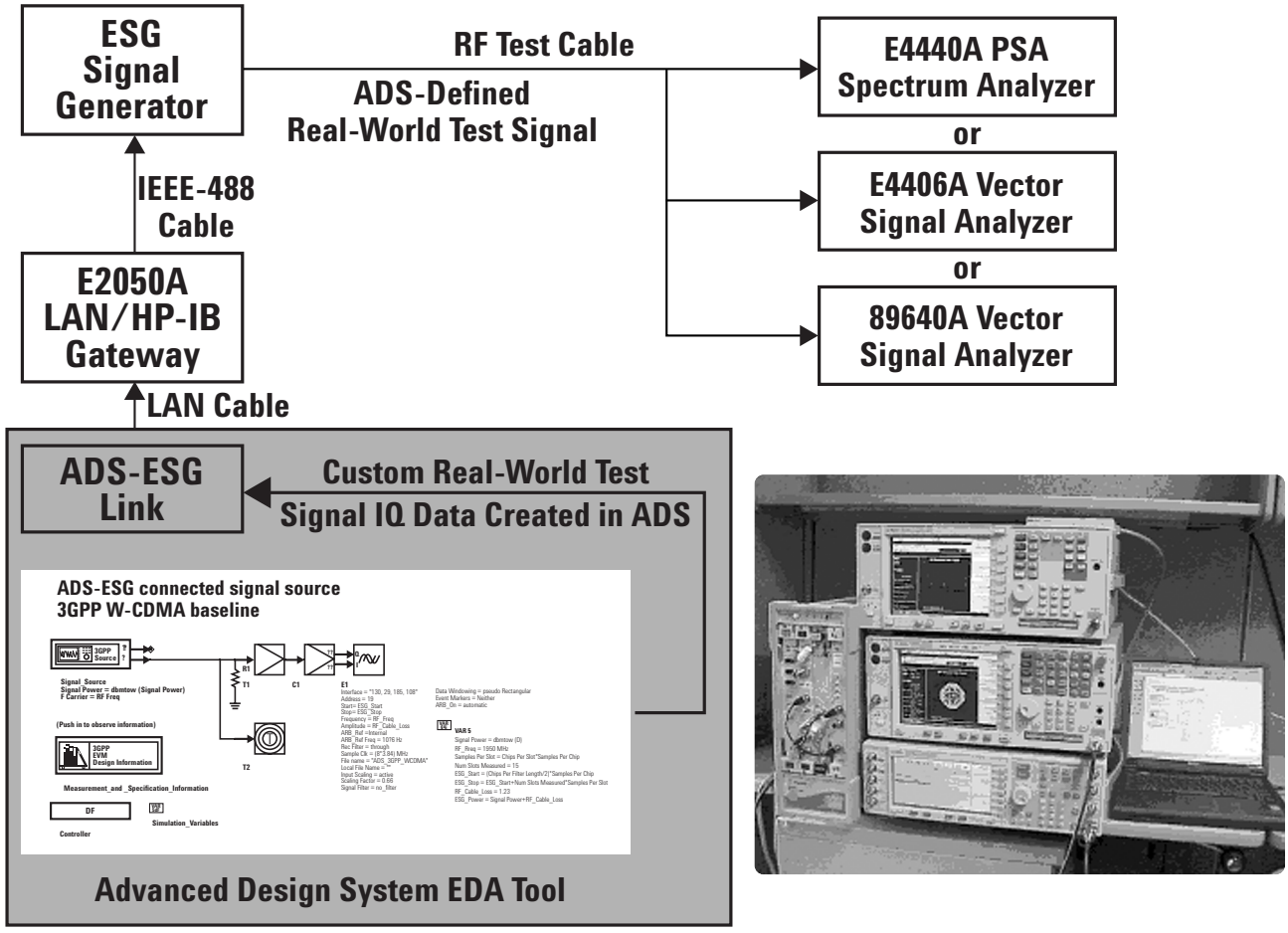


Figure 10. Basic Test Setup Showing Connectivity Between ADS and ESG (Left) and Bench Test Setup (Right), including the E4437B ESG (bottom), E4440A PSA (middle), E4406A VSA (top), 89640 VSA (left), Laptop with ADS (right). E2050A LAN/HP-IB Gateway is on top of E4406A VSA.

Step 4. Figure 11 shows each of the signal analyzers demodulating the baseline ADS-defined signal.

The measured results shown in figure 11 show that the baseline-connected signal source configuration is performing well. Some application examples are shown next, illustrating some of the distortions that can be modeled in ADS and created as a custom real-world test signal on the testbench using connected-source solutions. Each test case presents a simplified conceptual example, which can be extended and applied to real-world design verification tasks.

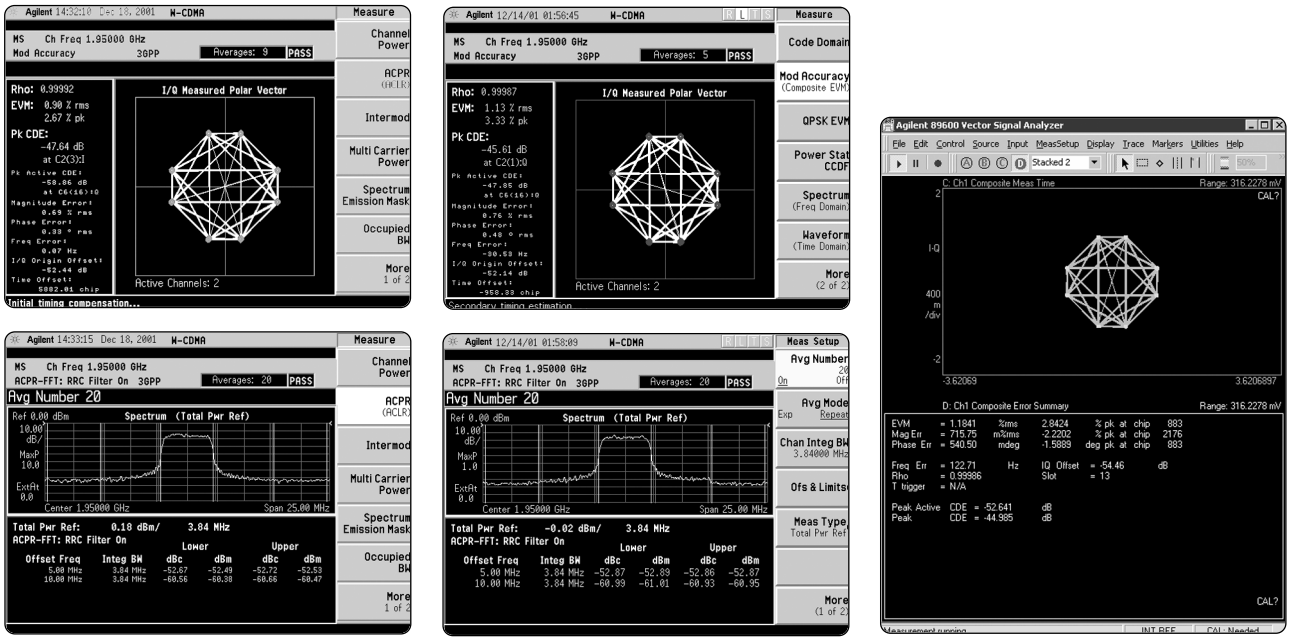


Figure 11. Baseline Example Case; EVM and spectral results of Agilent E4440A PSA, E4406A VSA, and 89640 VSA demodulating the "baseline" ADS 3GPP W-CDMA signal.

Note: With each of the signal analyzers the resulting EVM is relatively low, indicating good "baseline" signal quality with the ADS-ESG sink parameter settings selected. Note also that the measured EVMs agree within 0.3% (0.9% on the E4440 PSA , 1.13 % on the E4406 VSA, 1.18% on the 89640 VSA). The measured ACLRs agree within 0.3 dB between the E4440 PSA and E4406 VSA (not measured on the 89640 VSA).

Case Study 2:
Creating a Custom Real-World Test Signal Containing Amplitude and Phase Impairments

Case study 1 showed a baseline test case and corresponding measured versus simulated results, validating the baseline test setup. This case study expands on the baseline test case by introducing amplitude and phase impairments modeled in simulation to create a custom, real-world test signal on the testbench containing the simulated amplitude and phase impairments.

This case study follows the conceptual flow diagram shown below in figure 12 and shows how to create a signal in simulation with modeled amplitude and phase impairments and turn it into a real RF test signal on the test-bench. The custom real-world test signal (defined using ADS simulation) is then demodulated with a signal analyzer on the testbench and compared to simulated results for validation.

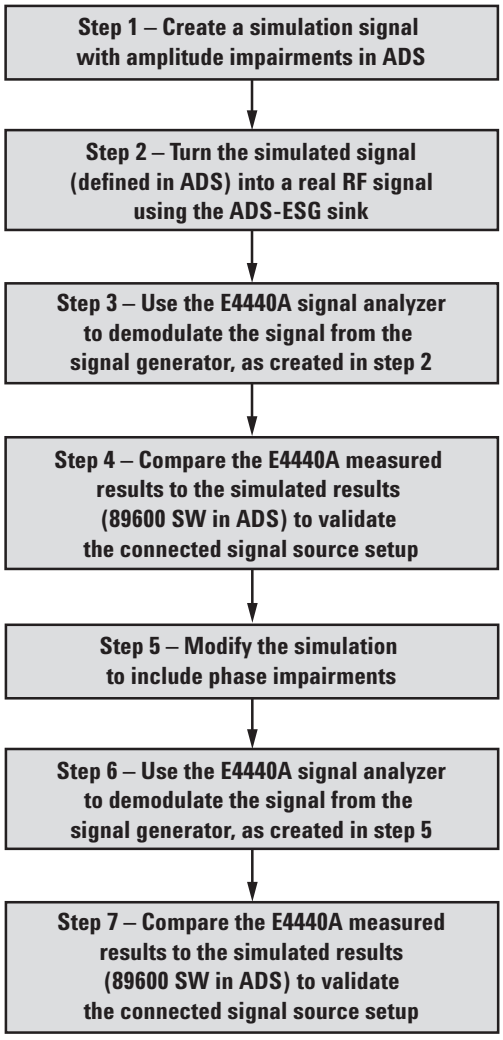


Figure 12. Conceptual flow for Case Study 2.

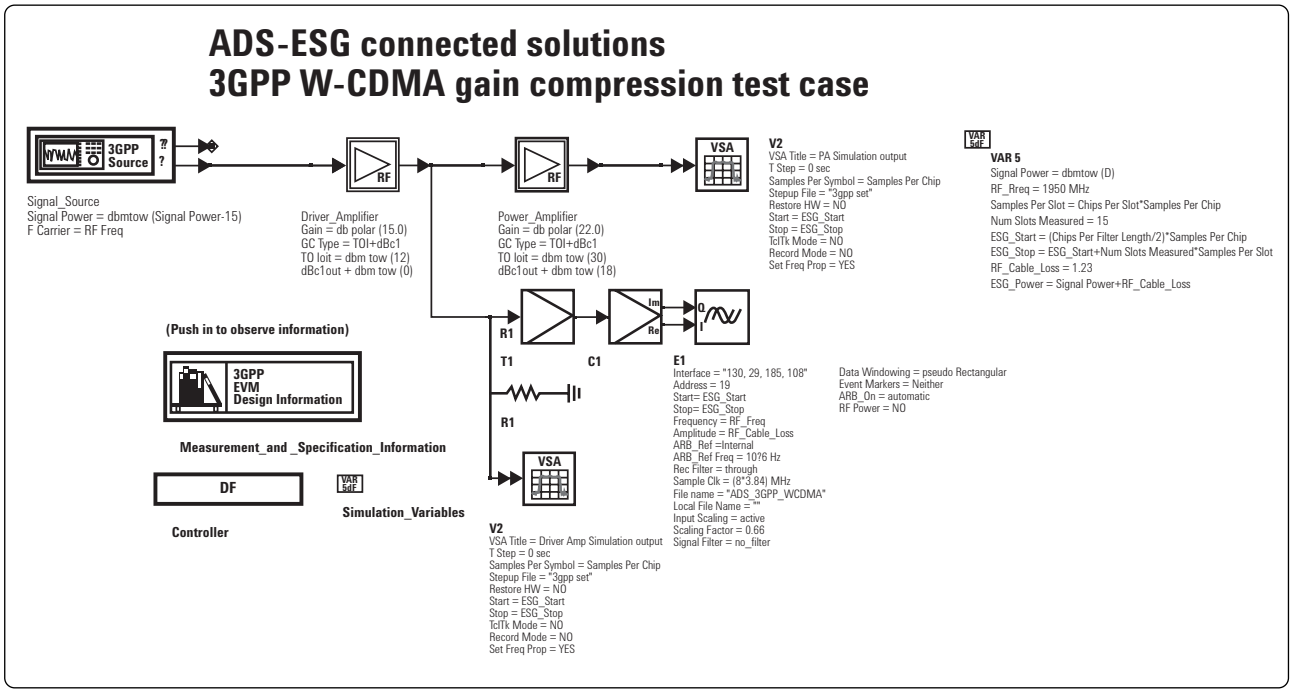


Figure 13. 3GPP W-CDMA example with gain compression.

Step 1. The schematic in figure 13 was created by copying and modifying the 3GPP W-CDMA baseline schematic to add a behavioral driver amplifier and a behavioral power amplifier. The ADS-ESG sink is connected to the input of the simulated power amplifier to emulate a test case in which a power amplifier is being tested on the testbench. A real-world test signal is needed at its input which reflects the amplitude distortions of the components driving it (such as an RFIC). In this conceptual example, a simple behavioral driver amplifier provides the modeled distortion in ADS.

Two 89600 software simulation measurement elements have also been added to the schematic. The 89600 software option 105 enables the 89600 software to be dynamically linked from within ADS with similar measurement algorithms and graphical user interface used when performing measurements on the testbench. An 89600 software simulation measurement element is connected at both the output of the driver amplifier and output of the power amplifier to view the relative distortion added by the simulated power amplifier.

The parameters of the 89600 software simulation measurement elements are set as shown in figure 14. The “Tstep” parameter is set to 0 sec, which allows the 89600 simulation measurement element to use an arbitrary timestep as detected at its input. A pre-configured setup file is used, which sets up the 89600 simulation measurement element for 3GPP W-CDMA mode with displays configured. The “Start” and “Stop” parameters are set to the same variables as the ESG sink start and stop parameters.

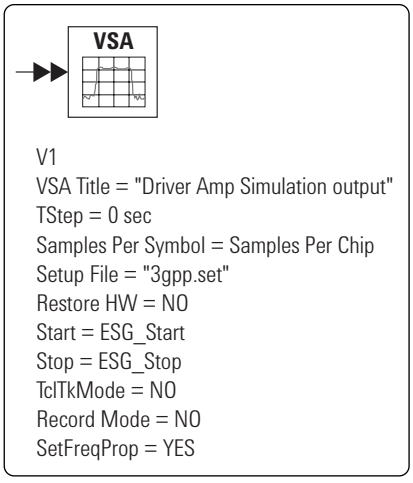


Figure 14. 89600 Software Simulation Measurement element parameter settings.

Step 2. The ESG sink parameters are configured with the same configuration discussed in case study 1. The simulation is performed, and the signal is downloaded into the ESG Arb.

Step 3. The ESG output is connected to the E4440A PSA input, as shown in figure15. The emphasis of this case study is to show how to create a real-world test signal with amplitude impairments. This real-world test signal could be used at a DUT.'s input for early verification testing (for example, modeling hardware not yet available for testing for early verification using the ADS-ESG sink). Figure 15 shows the output of the ESG, showing EVM and ACLR degradation resulting from the modeled driver amplifier. This real-world test signal, with the gain compression distortions resulting from the modeled driver amplifier in ADS, could be used as a real-world stimulus test signal if testing an actual power amplifier on the testbench.

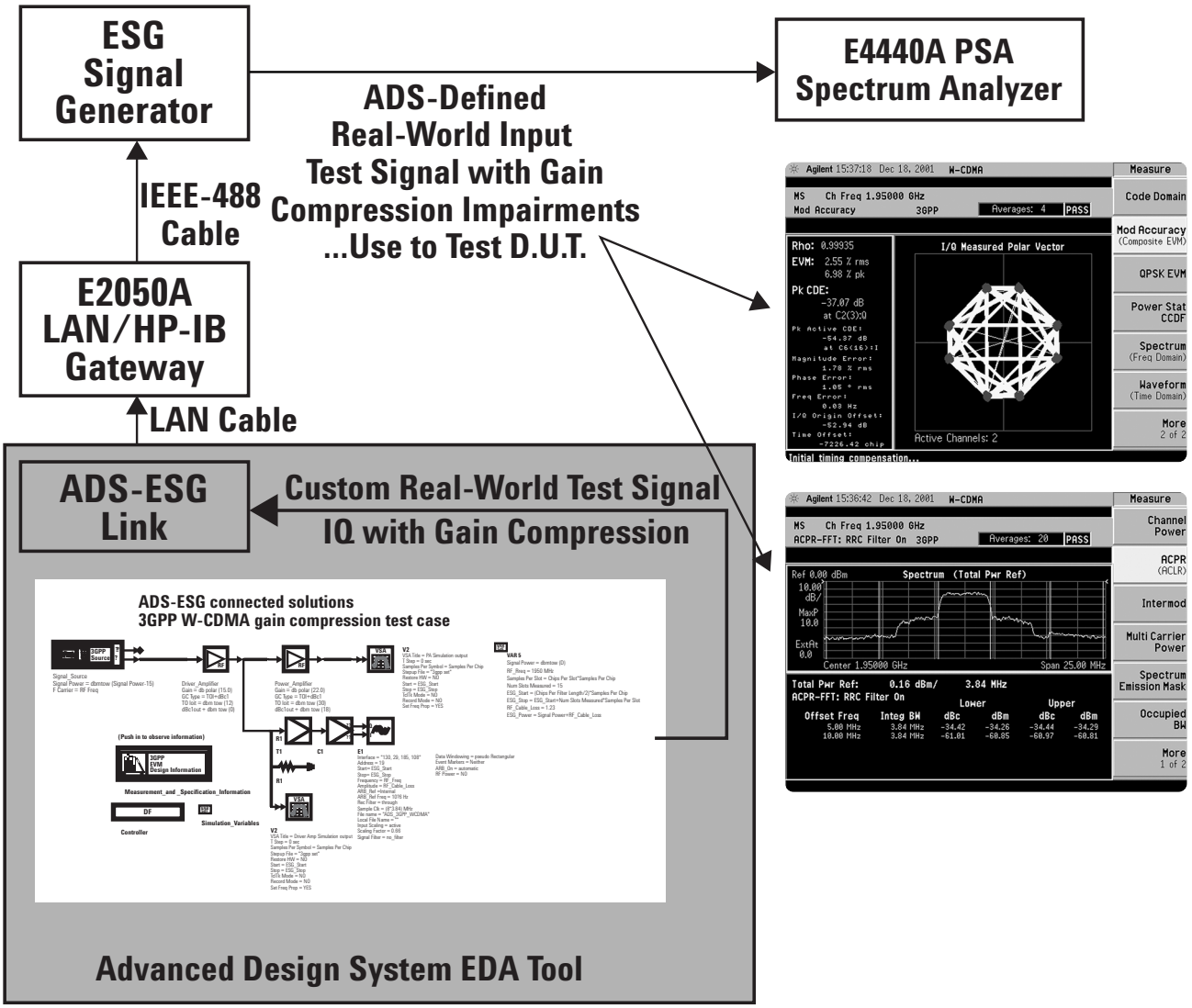


Figure15. Custom real-world test signal with simulated gain compression; Measured results using the E4440 PSA (right) showing degraded EVM of 2.55% from simulated amplitude impairments, relative to baseline as shown in Case Study 1.

Step 4. Figure 16 shows the simulated results, using the 89600 software simulation measurement in the ADS simulation environment. The upper right-hand simulation measurement display shows the sampled constellation and corresponding EVM result at the output of the simulated power amplifier. The lower right-hand simulation measurement display shows the spectrum with the spectral re-growth introduced by the simulated driver amplifier and the corresponding ACLR results.

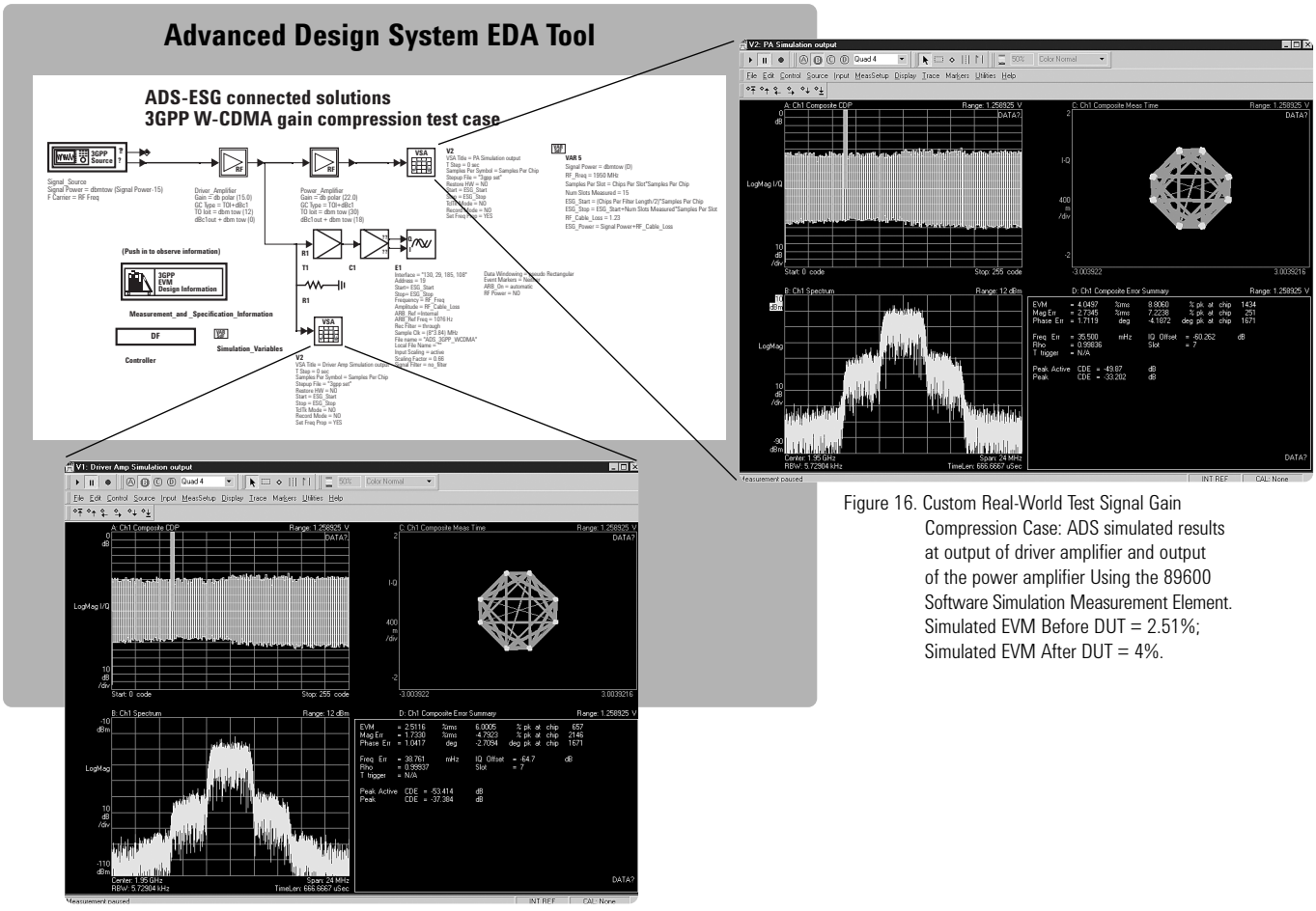


Figure 16. Custom Real-World Test Signal Gain Compression Case: ADS simulated results at output of driver amplifier and output of the power amplifier Using the 89600 Software Simulation Measurement Element. Simulated EVM Before DUT = 2.51%; Simulated EVM After DUT = 4%.

Note: The measured EVM results using the E4440 PSA show excellent agreement to the simulated EVM results (below) using the 89600 software simulation measurement element in ADS at approximately 2.51% (versus 2.55% measured using the E4440A PSA).

Including phase impairments

The current example shows how amplitude impairments resulting from a design can be modeled in ADS to create a real-world test signal on the testbench, containing the amplitude distortions introduced by the design.

Step 5. We now extend this example to include phase distortion by adding a narrowband filter behind the driver amplifier. The schematic shown in figure 13 is modified to include a 5th order bandpass Chebyshev filter with a 5-MHz, 1-dB bandwidth, which is the RF channel bandwidth for 3GPP W-CDMA. The resulting schematic is shown in figure 17.

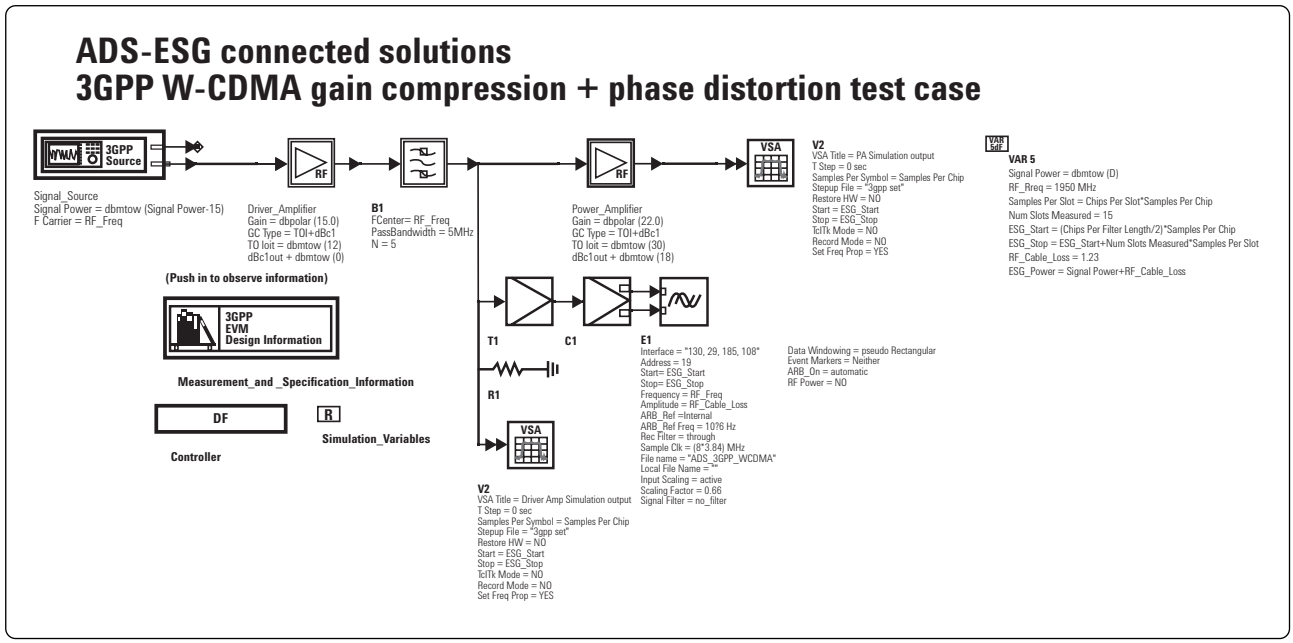


Figure 17. Modified design including bandpass filter.

Step 6. The simulation is performed and the output signal from the ESG is observed using the E4440A PSA as shown in figure 18. Figure 19 shows the corresponding simulated measured results from the amplitude and phase impairments modeled in simulation.

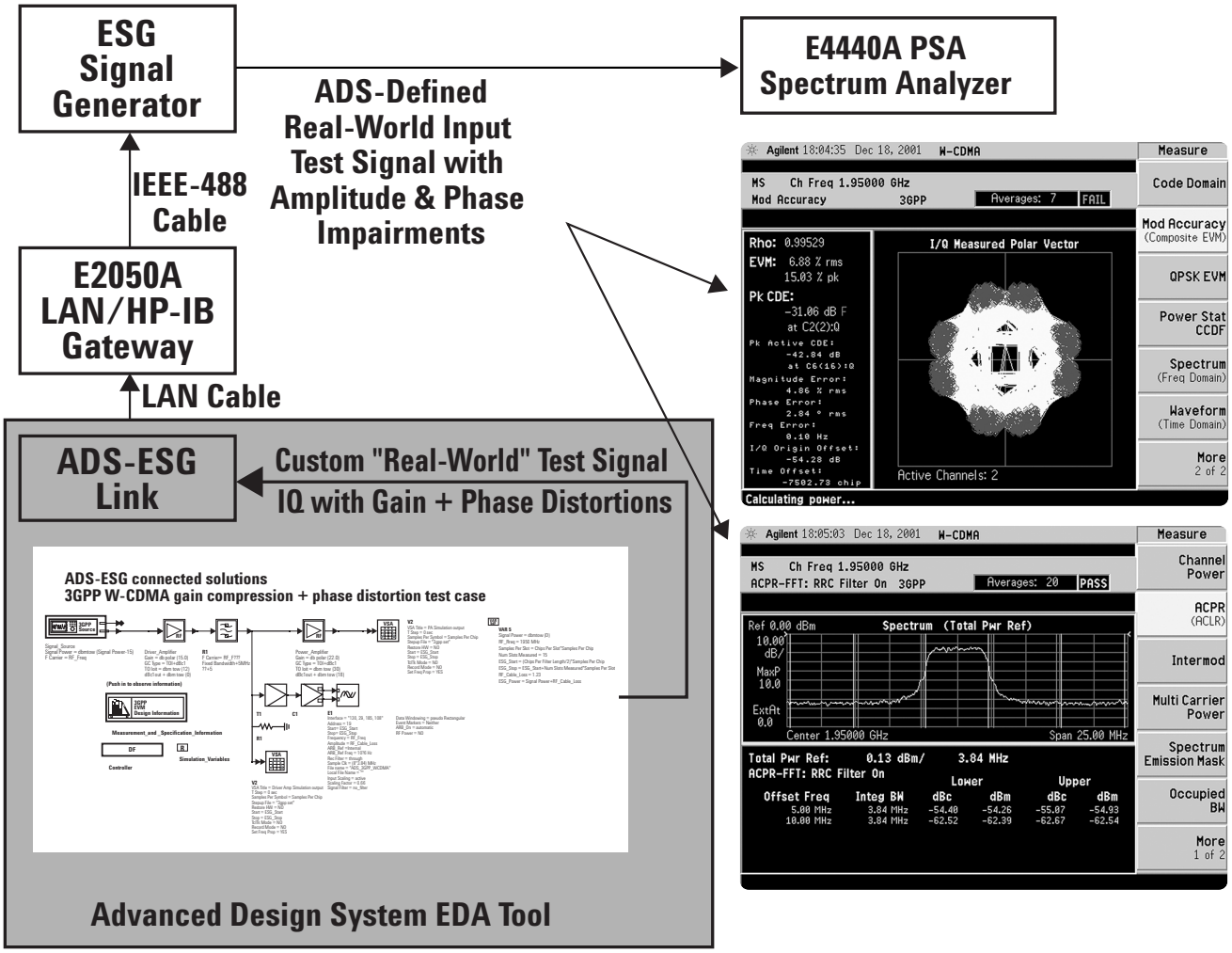


Figure 18. Custom real-world test signal with simulated gain compression and phase distortion; ADS-ESG Sink test setup and measured results showing degraded EVM of 6.88% from simulated amplitude and phase impairments relative to baseline shown in Case Study 1; ACLR has improved relative to the gain compression test case showing significance of using signal analyzer instead of spectrum analyzer.

Step 7. Figure 19 shows the simulated results in ADS using the 89600 software simulation measurement. Note that the EVM before the power amplifier is 6.67% and 6.9% at the output of the simulated power amplifier, implying that much of the EVM degradation may be occuring before the power amplier. This may difficult to determine on the testbench, if testing the power amplifier by itself; however, creating the real-world test signal by modeling the driver amplifier and filter may allow this effect to be measured on the testbench.

These simplified examples show how the connected signal source solutions can be used to model amplitude and phase distortions introduced by a design to create a custom real-world test signal on the testbench using the ADS simulation environment and the ADS-ESG sink. Missing hardware not yet available for test can be modeled in ADS and a representative real-world test signal can be created on the testbench using the ADS-ESG sink to help begin early verification testing before all of the hardware has been fabricated.

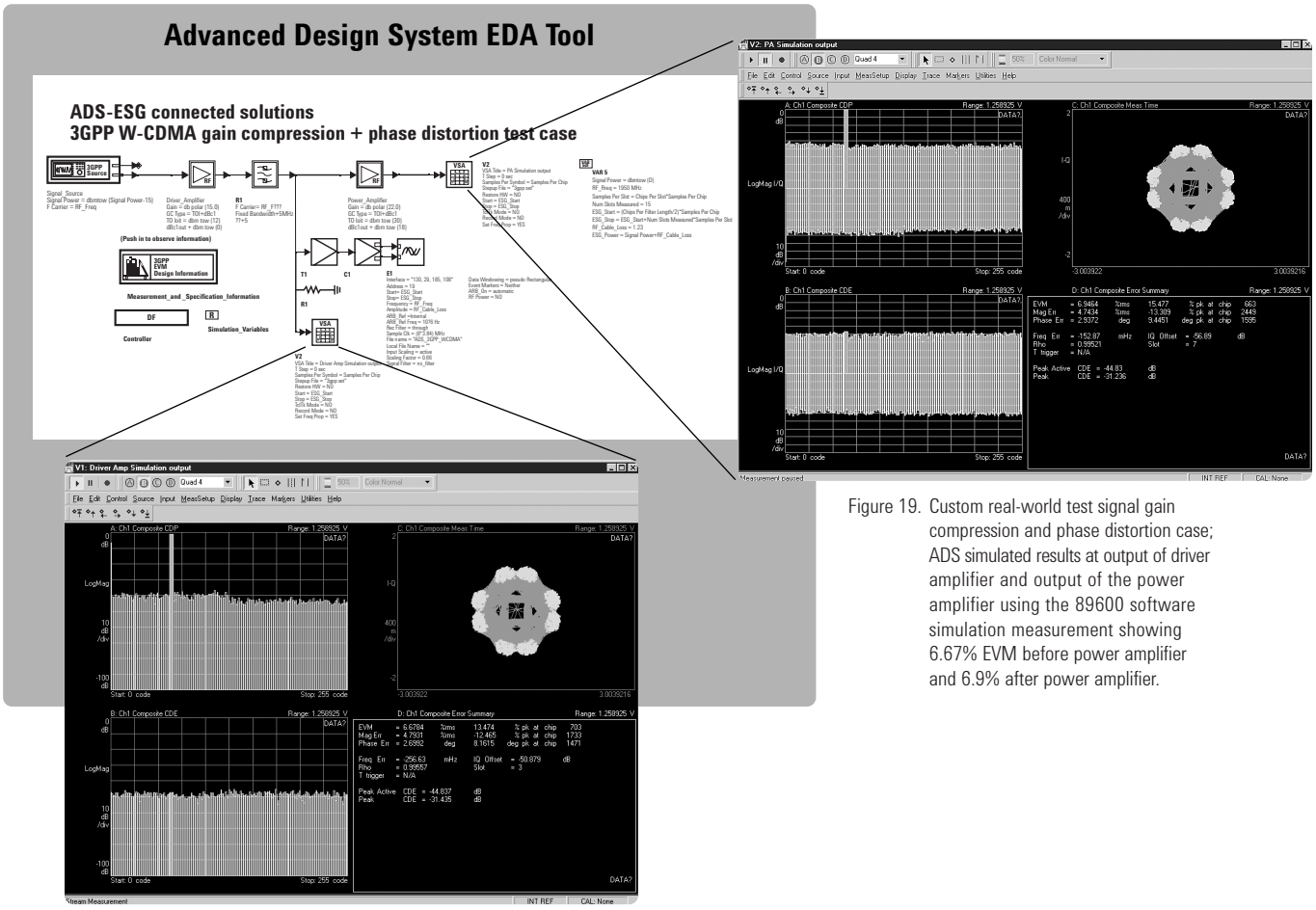


Figure 19. Custom real-world test signal gain compression and phase distortion case; ADS simulated results at output of driver amplifier and output of the power amplifier using the 89600 software simulation measurement showing 6.67% EVM before power amplifier and 6.9% after power amplifier.

Note: The measured EVM has degraded to 6.88% (versus 6.67% simulated), as a result of the phase distortion and inter-symbol-interference (ISI) introduced by the bandpass filter. Also note that the filtering has suppressed the out-of-band spectral re-growth which has improved the Adjacent Channel Leakage Ratio (ACLR), illustrating a design trade-off of improving the spectral performance at the expense of introducing InterSymbol Interference (ISI) which may degrade EVM. Note that performing a spectrum-only type measurement without digital demodulation would show the spectral performance improving, but not provide insight into the EVM degradation that that is introduced because of the ISI.

Excellent agreement was shown in this case study for simulated versus measured results.

Some potentially useful example applications include:

- Modeling an RFIC design (entire design or portions of) to test a mixer, driver amplifier, power amplifier, or some other DUT as evaluation parts return from fabrication, instead of waiting until all parts are available for test
- Evaluating re-using hardware with a preliminary modeled designs (for example, evaluating a filter or PA with a modeled RFIC design) to determine their combined performance
- Performing "what-if" scenarios on a DUTs measured performance by modifying the stimulus modeled in simulation (for example, will it meet specifications if a portion of a design is modified?)
- Creating simulation verification templates by modeling different stages in a design to facilitate individual component testing (for example, system engineer providing various ADS schematics to component designers to test individual components)
- Evaluating a proprietary signal format by modeling the signal in ADS (for example, creating a new, non-standard signal format in ADS and demonstrating its performance on the testbench)
- Performing RF testing, simulating the baseband functionality (for example, a Finite Impulse Response filter) in simulation to begin testing the impact on RF performance (for example, ACLR, EVM) before the baseband hardware is available

Case Study 3.
Creating a Real-World Test Signal Containing Baseband Impairments

Today's system design performance often depends on the combined performance of the baseband design as well as the RF design. In addition, fast time-to-market constraints may require that both the baseband and RF designs progress in parallel, even though design and testing of the individual sections may depend on one another (for example, coded BER, spectral mask from an FIR filter, and so on). This can provide a verification challenge, since all of the hardware (both baseband and RF) may be required before verification testing can begin. This case study will show a brief example to illustrate that baseband design impairments can be modeled in addition to RF impairments when creating real world test signals with connected signal source solutions. This case study follows the conceptual flow diagram shown in figure 20 and shows how to create a signal in simulation with modeled baseband impairments and turn it into a real RF test signal on the testbench. The custom real-world test signal (defined in simulation) is then demodulated with a signal analyzer on the testbench and compared to simulated results for validation.

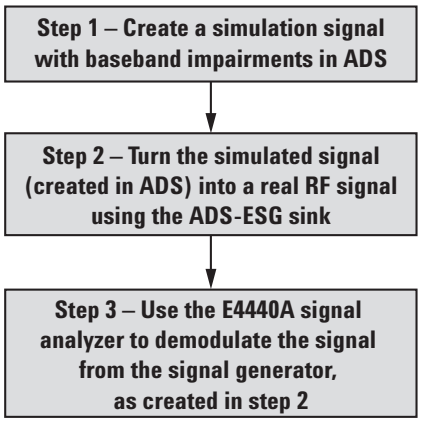


Figure 20. Conceptual flow diagram for Case Study 3.

Step 1. A 48-tap, fixed point, Finite-Impulse-Response (FIR) filter is designed in ADS with a finite bitwidth of 10 bits. The 3GPP W-CDMA Source and RF modulator sub-networks containing the fixed-point FIR filter are created as shown in figure 21. The floating-point RF modulator is de-activated and the fixed-point RF modulator (containing the fixed-point FIR filter) is instead used. The fixed-point FIR filters are used in-place of the behavioral RRC filters at the I and Q inputs of the RF modulator to simulate baseband impairments.

Step 2. The ESG sink parameters are configured with the same configuration discussed in case study 1 and case study 2. The simulation is performed and the ADS signal is downloaded into the ESG arbitrary waveform generator.

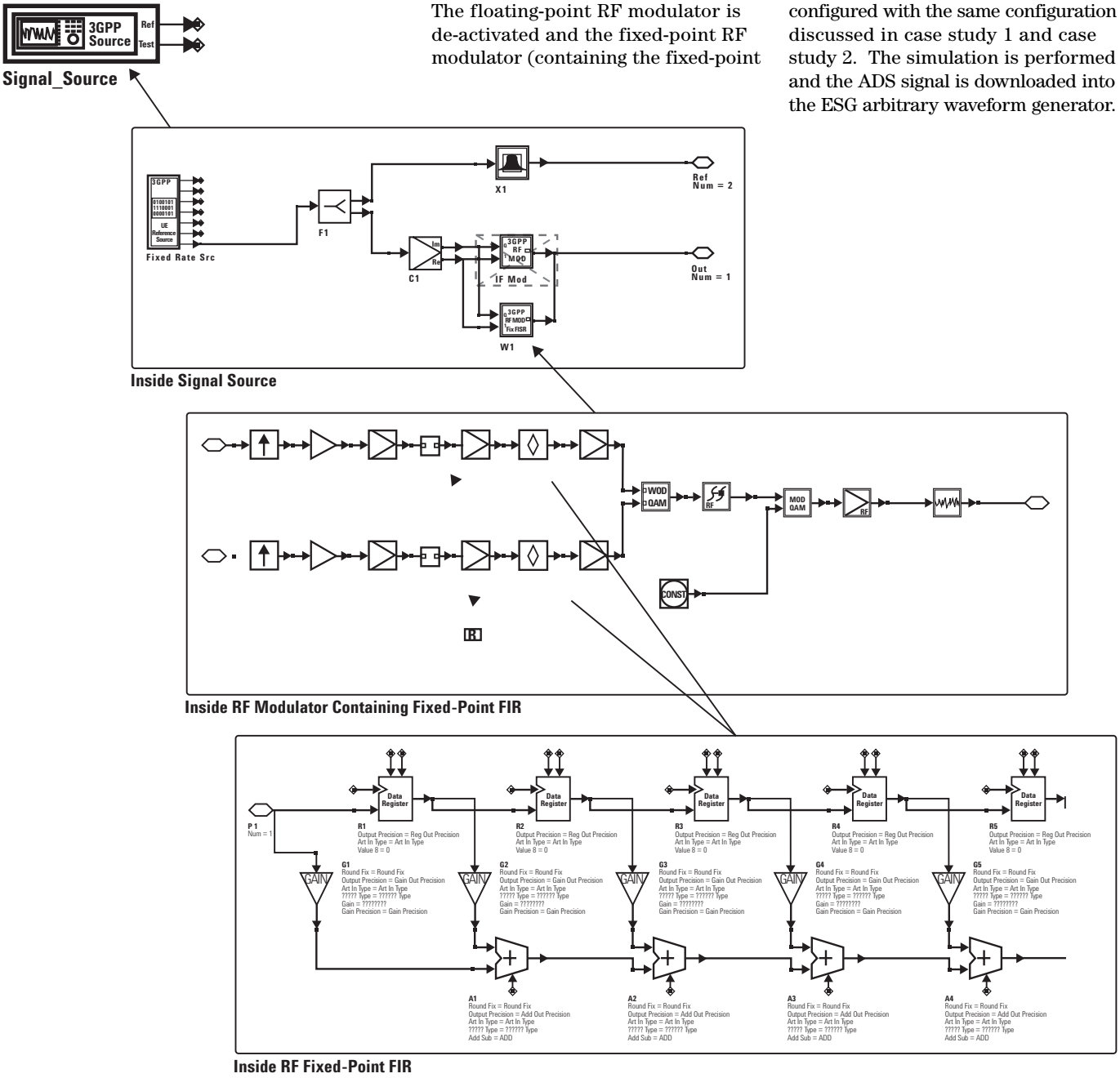


Figure 21. Modified 3GPP W-CDMA Signal Source with 10-Bit FIR Filter.

Step 3. The output signal from the ESG is observed using the E4440A PSA as shown in figure 22. Note that the measured EVM has degraded to 7.83% as a result of the baseband distortion introduced by the fixed-point FIR baseband filter in simulation. Also note, that the finite-bitwidth of the baseband filtering results in a non-ideal frequency spectral mask, which may impact spectral measurement test results of an RF DUT (such as ACPR/ACLR) if this signal was to be used as the input stimulus to a hardware DUT.

In summary, connected signal source solutions can be used to model distortions introduced by baseband designs to create a real-world test signal on the testbench for early verification testing in a parallel RF/DSP design cycle. Missing baseband functionality not yet available for RF testing can be modeled in ADS and a representative real-world test signal can be created on the testbench using the ADS-ESG sink to begin early verification testing before the baseband section is available for testing. Some examples of applications for which this could be useful are:

- Verifying mixed-signal RF performance (ACLR, EVM, Spectral Mask, and so on) with baseband effects considered in a parallel RF/ baseband design cycle.
- Partitioning baseband requirements (for example, FIR performance) at a combined baseband/RF system level by modeling various baseband scenarios in ADS and testing on the testbench with RF hardware and the ESG/VSA.
- Verifying mixed-signal performance by modeling RF impairments in ADS and testing baseband hardware on the testbench.

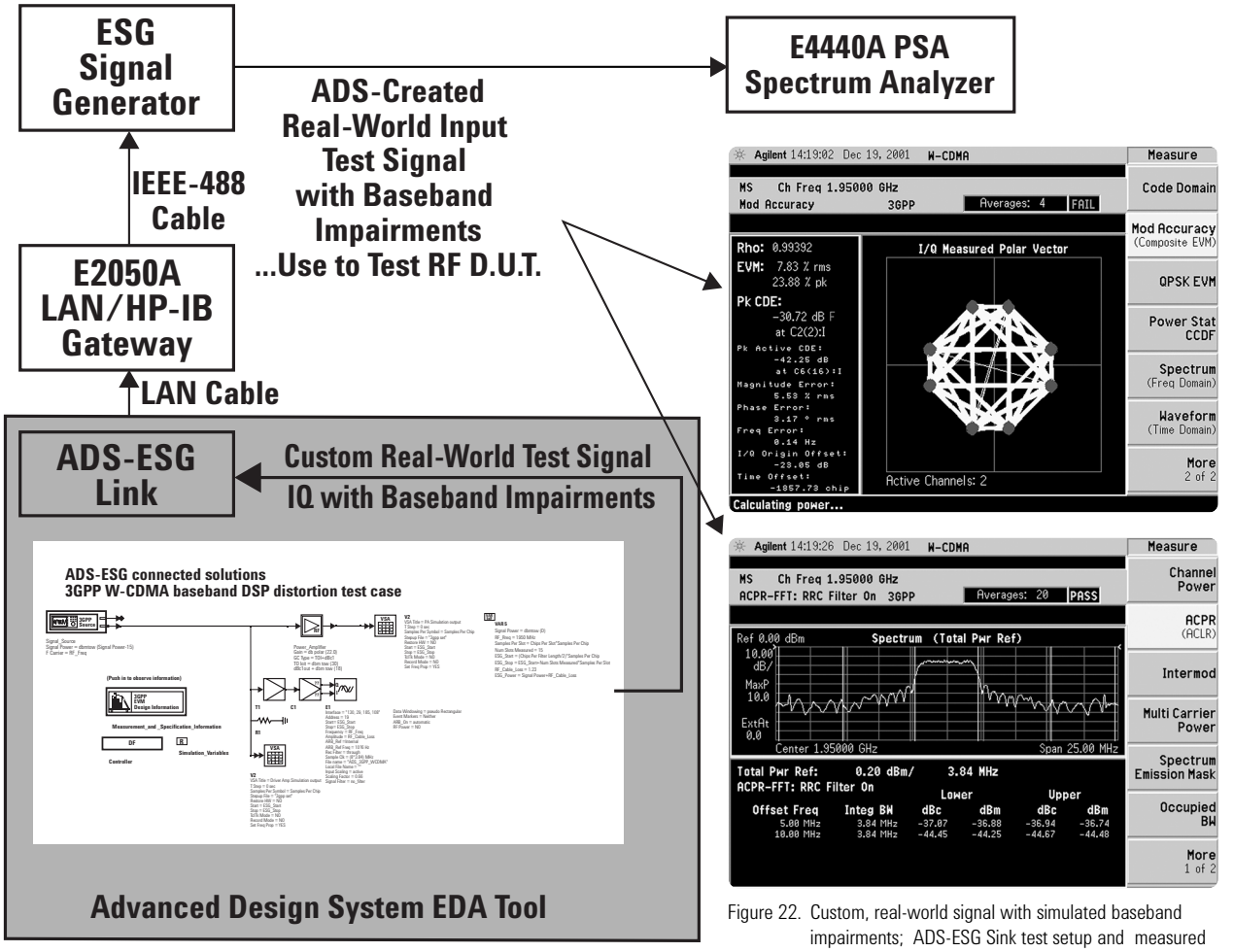


Figure 22. Custom, real-world signal with simulated baseband impairments; ADS-ESG Sink test setup and measured results using the E4440 PSA, showing 7.83% degraded EVM resulting from baseband filter and degraded spectral performance from baseband filter, relative to baseline shown in Case Study 1.

Using Connected Signal Analyzer Solutions to Measure a Signal on the Test Bench and Bring it Back into Simulation

This section discusses connected signal analysis capability. This connection allows powerful signal analysis testing to combine with the flexibility of simulation, which allows measured DUT signals on the testbench to be read into simulation for further analysis and post-processing.

This capability involves using the 89600 software (version 3.0 or later with Option 105) simulation source element to read measured IQ data from the 89640A VSA, E4406A VSA, or E4440A PSA on the testbench back into the ADS simulation environment for further analysis in simulation.

The fundamentals of setting up the 89600 software simulation source (discussed in this section) are applied in example case studies presented in the next section of this application note.

ADS Connected Signal Analyzer Solutions

The previous case studies showed an 89600 software simulation measurement being dynamically linked from within ADS (for example, figure 19). Version 3.0 (or later) of the 89600 software with option 105 also offers simulation source capability in addition to the simulation measurement capability. This simulation source capability enables the I & Q signals measured from Signal Analyzer hardware on the testbench to be brought back into the ADS simulation environment to be used as a simulation stimulus signal for a design modeled in the ADS simulation environment. Specifically, the I & Q from an Agilent 89640A Vector Signal Analyzer, E4406A Vector Signal Analyzer, or E4440A Performance Spectrum Analyzer can be brought back into ADS using the 89600 software simulation source running from within ADS.

This section discusses the fundamentals of setting up the 89600 software simulation source to help show you how to read measured signals back into simulation with Agilent connected solutions. The 89600 software simulaton source element and its parameters discussed first.

The 89600 Software Simulation Source Element and its Parameters

Figure 23 shows the 89600 software simulation source element connected to a resistor and an 89600 software simulation measurement element in ADS.

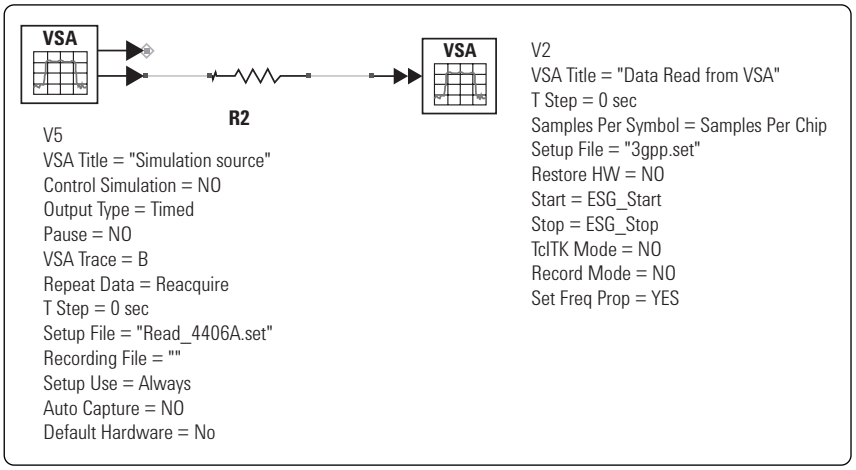


Figure 23. 89600 Software Simulation Source Element Connected to an 89600 Software Simulation Measurement Element in ADS.

89600 Software Simulation Source Parameters

The 89600 software simulation source has various parameters:

1. **“VSATitle”** Parameter. This parameter defines the text labeling to appear at the top of the measurement display when the simulation is launched.

2. **“ControlSimulation”** Parameter. The simulation duration in the ADS DSP schematic window can be controlled from sources or sinks in the schematic window. This parameter defines how long this signal source produces data and whether the source will control the simulation. When this parameter is set to “NO,” the signal source keeps the simulation running long enough to cover one pass through the data. When this parameter is set to “YES,” the signal source runs for the duration defined by the sink(s) controlling the simulation duration.

3. **“Output Type”** Parameter. The DSP schematic window supports a variety of different signal types. The “Timed” signal format is most typically used for “RF” signals represented with a modulated carrier frequency.

   - *Timed* - Timed data is output at the 89600 center frequency and time step (see TStep below). The data is complex or baseband, depending on the 89600 zoom state. Requires time domain measurements from the 89600. Example 89600 trace data type: "Main Time."
   - *Frequency* - Spectrum data is output as pairs of complex numbers. The first number is the real frequency (the imaginary part is zero), and the second number is the complex voltage at that frequency. You can connect a Distributor2 to the VSA89600Source data port to separate the signal. Requires frequency domain measurements from the 89600. Example 89600 trace data type: "Spectrum."
   - *Demod Errors* - Demodulation error data is output as sets of floating point values. The number of values and required 89600 configuration varies with demodulator type.
   - *Complex Scalar* - Complex numbers are output. If the 89600 measurement data is real-valued, the imaginary part of the output values is zero. Example 89600 trace data type: "Error Vector Time" in Digital Demod mode.
   - *Float Scalar* - Floating point numbers are output. Requires real-valued 89600 measurement data. Example 89600 trace data type: "IQ Mag Error" in Digital Demod mode.
   - *Integer Scalar* - Integer numbers are output. Requires real-valued 89600 measurement data. Useful for sourcing demodulation symbols when the 89600 trace data type is "Syms/Errs."

4. **“Pause”** Parameter. The “RecordingFile” parameter can be used to automatically recall a recording into the 89600 during simulation start-up. If “Pause” is set to YES, the setup file and recording files are loaded before the Pause dialog is displayed.

5. **“VSATrace”** Parameter. Defines which trace will provide measurement data.

6. **“RepeatData”** Parameter. Defines how data is transferred into ADS from the hardware-based measurement. “Single Pass” supplies data from a single measurement. “Repeat” acquires a single measurement and repetitively sources it into the simulation. “Re-acquire” repeatedly acquires and sources new measurements. The data across measurements in the “Repeat” and “Re-acquire” modes are not time-continuous.

7. **“Tstep”** Parameter. Specifies the time step associated with the simulation source data being output. This should generally be set to the same time step being used in the ADS simulation. A value of 0 seconds produces data with the timestep set by the 89600, based on the frequency span selected. This parameter should be set to value equal to or larger than the timestep associated with a recorded file when reading from a previously created recorded file (effectively downsampling the data if set to a larger value).

8. **“SetupFile”** Parameter. This parameter can be used to automatically recall an 89600 setup file during the simulation start-up and is useful for setting up the 89600 configuration when repetitively performing simulation. The setup file can be created by configuring the 89600 software simulation source as desired, and then selecting File > Save > Save Setup... on the 89600 menu bar and specifying the name of the *.set file to be saved in the /data subdirectory of the ADS project. Setup files in locations other than the /data subdirectory can also be specified by providing the relative path (for example, ../../../ filename.setup) or absolute path (for example, C:/my_dir/filename.setup) of the .setup file. The “SetupUse” parameter defines how the setup file is to be recalled. If “Pause” is set to YES, the setup file is loaded before the Pause dialog is displayed.

9. **“RecordingFile”** Parameter. This parameter defines whether new measurement hardware data should be gathered or if previously recorded data is used as the simulation signal source. If no recording file is specified, then measurement hardware data is gathered. Recorded (.sdf) files are useful for performing repetitive simulations when the measurement hardware data is not expected to change from one simulation to the next or when it is desirable to perform simulation without the presence of measurement hardware. If “Pause” is set to YES, the recording file is loaded before the Pause dialog is displayed.

10. **“SetupUse”** Parameter. Defines when an 89600 setup file (specified in the SetupFile parameter) will be recalled. Options are:

    - Always - recall setup file on every simulation run
    - Once - recall setup file only when 89600 is started
    - No - do not recall setup file

11. **“AutoCapture”** Parameter. Setting this parameter to YES will automatically initiate a capture recording of the hardware input data when the simulation is launched. The model begins sourcing the data into the simulation when the capture is complete. Time-based measurements can be continuous, except for wrapped values when a playback loop occurs. Recording length can be controlled via an 89600 setup file.

12. **“DefaultHardware”** Parameter. If set to YES the 89600 automatically selects an appropriate hardware configuration. Otherwise the 89600 will use previously selected hardware settings.

Selecting Signal Analyzer Measurement Hardware

The 89600 software must first be installed before selecting signal analyzer hardware. Installation notes which describe installing the 89600 software and configuring the 89600 software for signal analyzer hardware can be found at **www.agilent.com/find/89600**, by selecting the applicable product category, and then selecting Manuals, Guides, and Service Notes.

When the 89600 software is started (Start > Programs > Agilent 89600 VSA > Vector Signal Analyzer), it retrieves supported hardware information from the resource manager table and determines what the installed hardware configuration is. The Select Hardware dialog box (Utilities > Hardware) of the VSA displays this information. The devices are grouped and listed by their hardware type, as indicated by the tab header. The information is tailored to the specific device and includes address, location, and name (or description).

Run the 89600 analyzer

1. Start the analyzer by double-clicking the appropriate icon on your desktop or by clicking **Start, Programs, Agilent 89600 VSA, Vector Signal Analyzer**.

2. Click **Utilities, Hardware**. Verify that the Simulate hardware box is unchecked.

3. Under ADC1 tab select the address that corresponds to the Agilent PSA. Be sure that nothing is selected on the other tabs in the Select Hardware window.

Putting it All Together: Combining Connected Signal Source and Signal Analyzer Solutions

This section applies the fundamentals of combining connected signal source and connected signal capabilities to define a signal in simulation, turn it into a real RF test signal using the connected signal source capability, and bring it back into simulation for further analysis.

Case Study: Performing a Connected-Solutions Coded BER Measurement

One of the most critical performance metrics in today's digital communications systems is BER (Bit Error Rate). Unfortunately, it is also can be one of the last verification tests to be performed because it typically requires both the RF and baseband hardware to be available for testing. The RF hardware can add impairments such as Intersymbol Interference (ISI), thermal noise, phase noise, and other impairments, which may impact the BER performance of the system. The baseband hardware, on the other hand, can also impact BER performance...an example would be the coding gain offered by algorithms implementing Convolutional coding or Turbo coding. Because of its importance as a performance metric and its dependencies on both the baseband and RF performance and risks associated with integrating the two together, it can be desirable to verify the BER performance as soon as possible. Furthermore, it might be useful to test the performance of a system with environment impairments such as fading and multi-path.

This case study illustrates how an Agilent connected solutions coded BER measurement can be performed to facilitate early verification testing of a design. It uses a signal flow in which a signal is defined in simulation, turned into a real RF test signal using connected signal source capability, and measured with the 89640A VSA signal analyzer. The signal is then recorded, and brought back into simulation using connected signal analysis capability to perform a connected solution coded BER measurement in simulation. The conceptual flow diagram is shown in figure 24 and the case study flow is shown in figure 25.

Conceptual signal flow for connected solutions BER

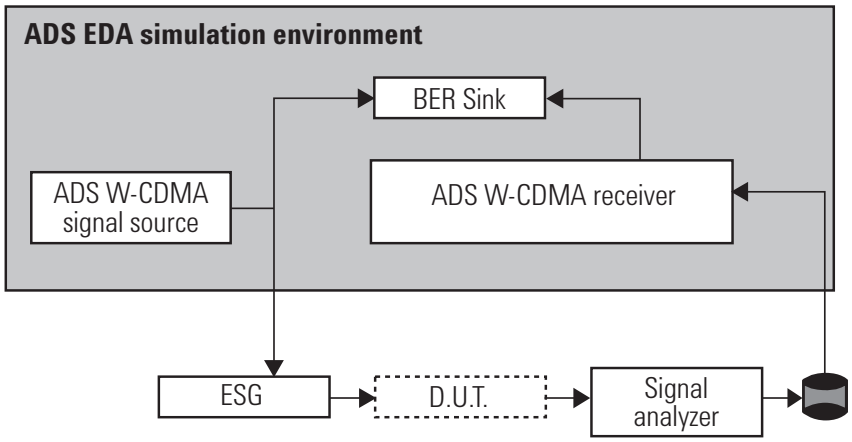


Figure 24. Conceptual flow diagram for a connected solution BER measurement.

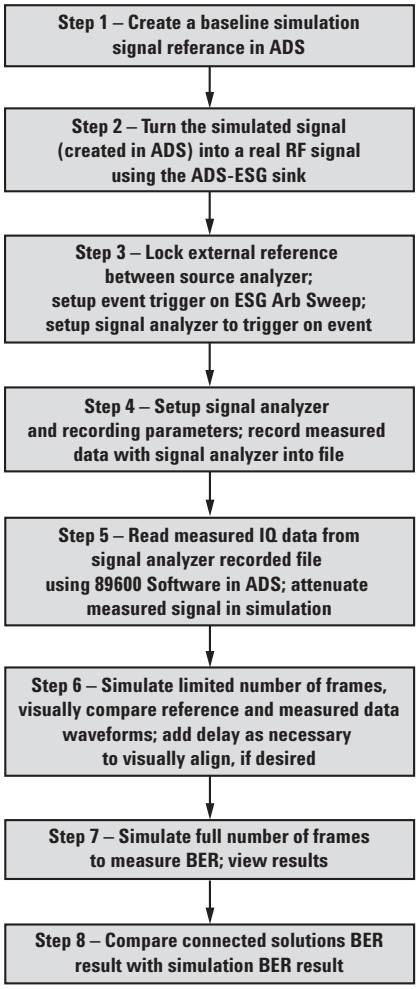


Figure 25. Case study flow.

Step 1. An ADS schematic is created as shown in figure 26. This schematic was created by copying and modifying the WCDMA3G_BS_Rx_prj project, which is included with the ADS 3GPP W-CDMA design library (E8875A/AN).

Notice that the ADS 3GPP W-CDMA signal source is different than the ADS signal source used in previous case studies. This is because the source, which was used in the previous case studies, did not expose pins for the reference data bits. Access to the reference data bits, however, is required to simulate BER for comparison to the measured data bits, so this source is instead used. This source is also used for compatibility with the current ADS 3GPP W-CDMA receiver.

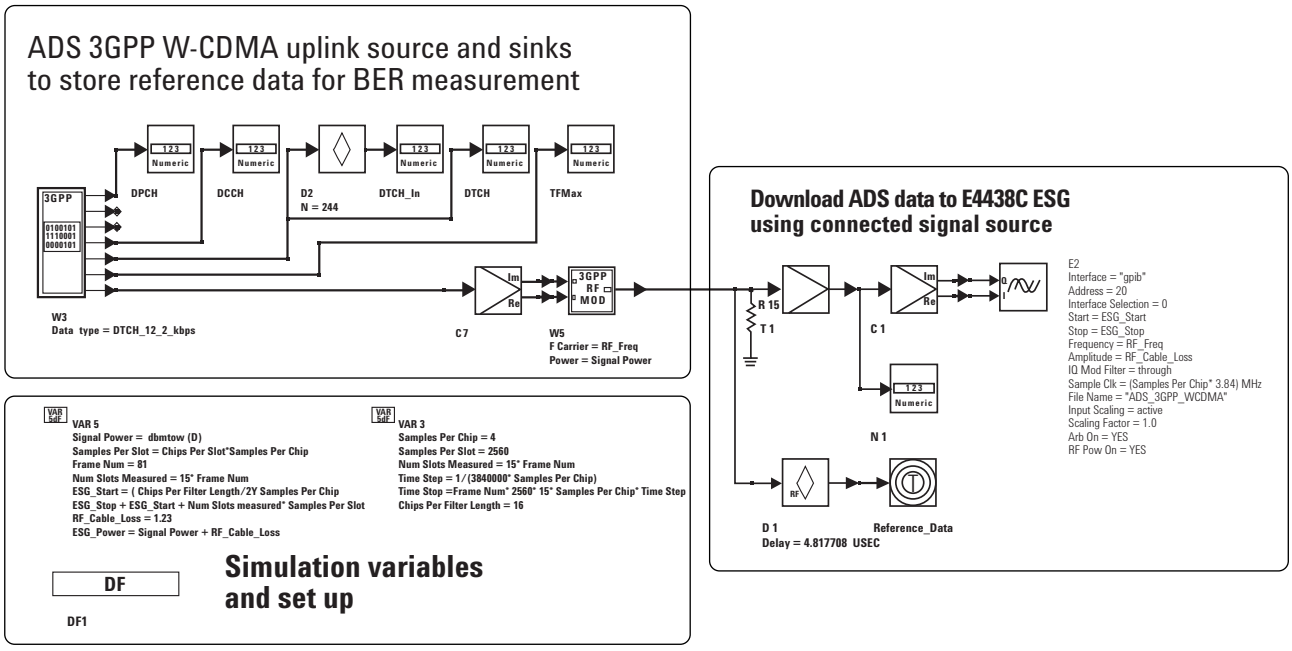


Figure 26. Baseline Connected Solution BER Reference Schematic with ADS-ESG Sink.

A close-up view of the simulation signal source portion of the reference schematic and the simulation setup variables is shown in Figure 27. Numeric sinks are connected to the various data output pins to store the reference data into a simulation dataset. These will later be used and read by the ADS 3GPP W-CDMA receiver to use as the reference data for the BER measurement. The sink labled DPCH records the physical channel data to be used in the physical uncoded BER measurement. The sink labeled DTCH records the Dedicated Traffic Channel (DTCH) data bits to be used in the coded BER measurement. The DTCH data bits are the primary data bits which are of interest for this coded BER measurement. In addition, there is a sink labeled DTCH_In, which is delayed by 244 samples (bits) so that the original reference data bits can later be overlaid with the demodulated data bits recovered from the measured signal for a visual comparison of the reference and measured data bits. The ADS 3GPP W-CDMA receiver delays the output data by one frame, which is 244 samples (bits) for the reference channel setting used in this case study.

Notice that 81 frames of data are specified in the simulation setup (see “Frame Num = 81” in the VAR 5 variable block). The actual number of frames to be considered in the simulation is 80 frames, or one less frame than specified. This is due to the one-frame delay just discussed in which no data is output from the ADS 3GPP WCDMA receiver until one frame later.

A close-up of the ESG sink setup is shown in figure 28. The total number of samples downloaded into the E4438C ESG arbitrary waveform generator can be calculated as follows:

80 frames x 15 timeslots/frame x 2560 chips/timeslot x 4 samples/chip = 12,288,000 samples

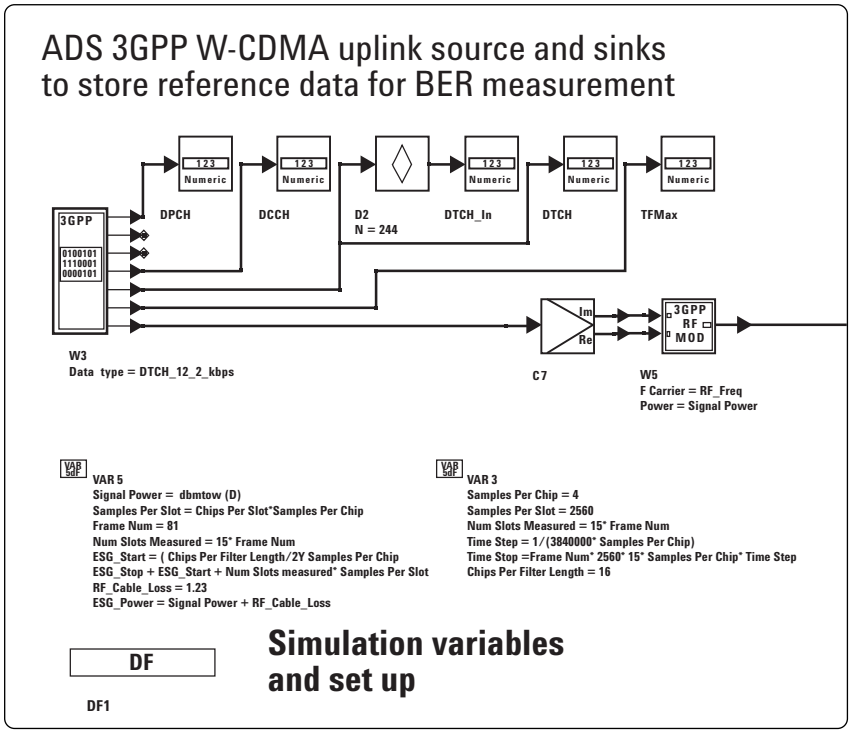


Figure 27. Close-up View of ADS Simulation Signal Source and Simulation Setup.

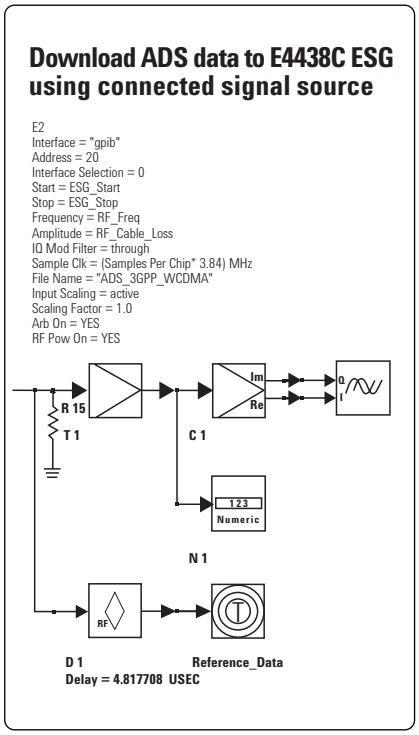


Figure 28. Close-Up View of ADS-ESG Sink.

Step 2. The simulation is run to download the ADS-defined signal source data into the E4438C ESG arbitrary waveform generator. The actual download of data may take some time, even after the E4438C ESG screen shows 100 % complete. Please wait for this status message to be dismissed from the E4438C screen before continuing. *Note that the PC should have 1 GB or more of virtual memory allocated to download the ADS-defined signal to the E4438C ESG.*

Step 3. Setting up the Signal Analyzer to Record the Measured Data. The E4438C and 89640A VSA are setup as shown in figure 29.

The 10 MHz references are locked together between the E4438C ESG and 89640A VSA. The Event 1 output of the E4438C ESG is connected to the Trigger input on the 89640A VSA.

To enable the ADS-defined waveform, select the following on the front panel of the ESG:

Local > Mode > Dual Arb > Select Waveform > "ARBI:ADS_3GPP_WCDMA"

An event marker is then turned on at the beginning of the Arb sweep by pressing the following keys on the ESG front panel:

Local > Mode > Dual Arb > Waveform Segments > Store > Waveform Utilities > Set Markers > "Set Marker On First Point"

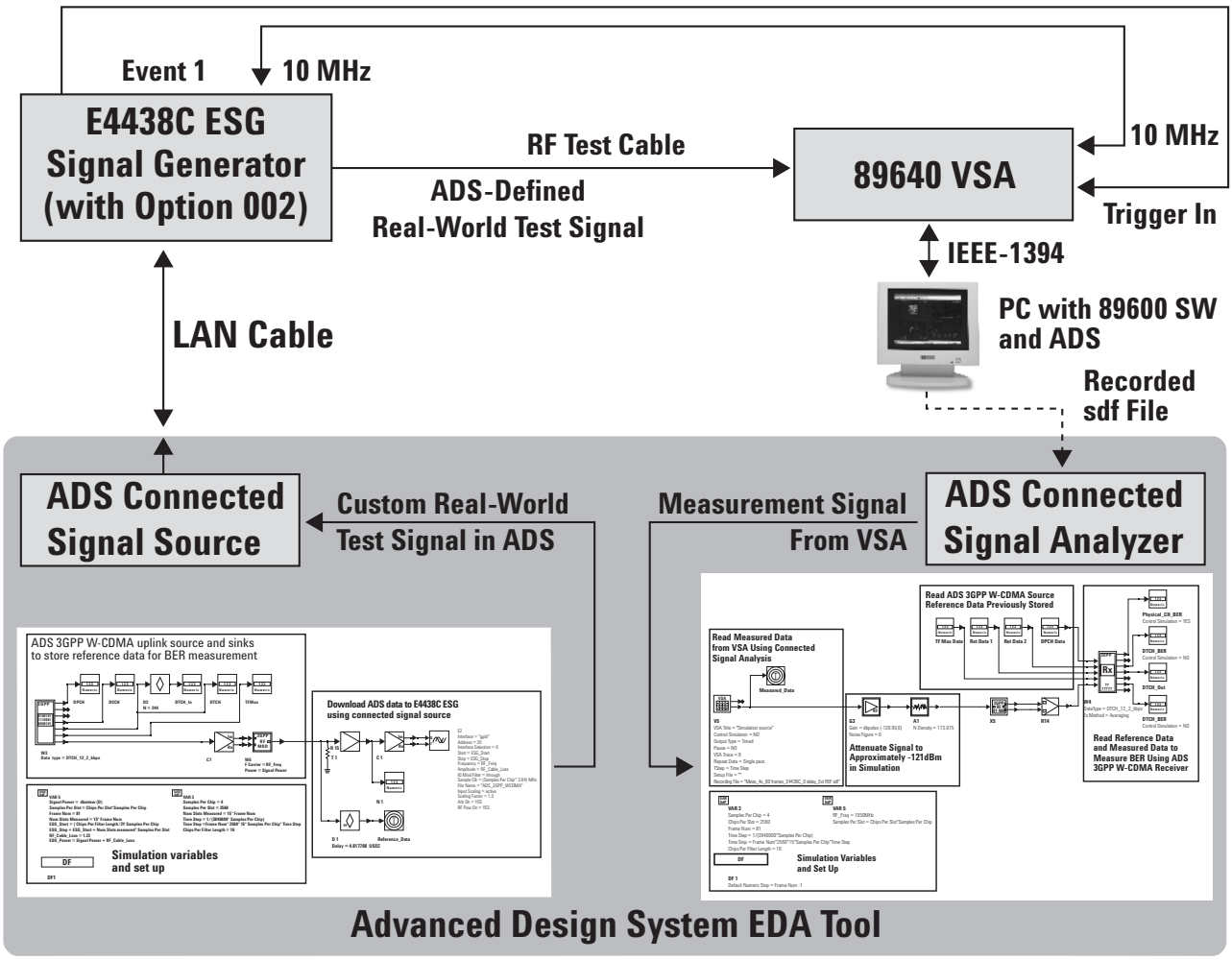


Figure 29. ADS Connected Solutions BER Test Setup.

Note: Proper triggering on the E4438C ESG event 1 marker output requires that the 89640A VSA utilizes a recent version of the E1439 module with TTL level triggering.

Note: PC should have 1 GB or more of virtual memory allocted to download the ADS-defined signal to the E4438C ESG.

Step 4. When the Arb waveform on the ESG is activated and the event marker is set for the Arb sweep, the 89640 VSA is next configured to capture the measured signal on the testbench. From the pull-down menus on the 89640 select Input > Trigger > Type > External TTL. This synchronizes the VSA measurement with the beginning of the ESG Arb sweep. Next, select MeasSetup > Frequency and set the Frequency Span to 15.36 MHz and set the center frequency to 1.95 GHz. The frequency span is set to 15.36 MHz, which corresponds to 1/timestep of the ADS signal downloaded into the ESG arb. This allows the recorded measured signal to be read back into ADS with the same ADS simulation timestep used to create the original signal. The 89640 VSA should now be measuring data and can be configured to record the measured data. To do this, select Input> Recording and set the recording length to 810 mS. 810 ms is selected because 80 10 mS frames of data of ADS data was downloaded into the ESG Arb. 810 mS of recorded data should be more than adequate to fully capture all of the ADS data. Start the recording by pressing the Record button. (Note that although the 89640 VSA data can be read into ADS without first recording it, a recording is desirable for BER applications because it will result in a time-continuous data stream when the file is read back into ADS).

A record status box shows the status and the completion of the recording. A temporary recording file is created; select File > Save> Save Recording... to save the recording to a permanent file. Select the SDF (Export) format, and type in the desired name of the *.sdf file. The file is saved in the/data subdirectory of the ADS project directory by default.

Step 5. The schematic to measure BER is shown in figure 30. The 89600 software simulation source is configured to read the previously recorded measured data. The measured signal is then attenuated in simulation to a level of –121 dBm, which is the basestation receiver sensitivity level defined in the 3GPP specifications. The attenuated measured signal is then demodulated to remove the carrier frequency and input into the ADS 3GPP WCDMA receiver to be used as the test signal for the BER measurement. Numeric signal generators are also configured to read the previously stored reference data from the ADS 3GPP simulation signal source. These are also input into the ADS 3GPP WCDMA receiver to be used as the reference data for the BER measurement.

A close-up of the 89600 software simulation source setup is shown in figure 31.

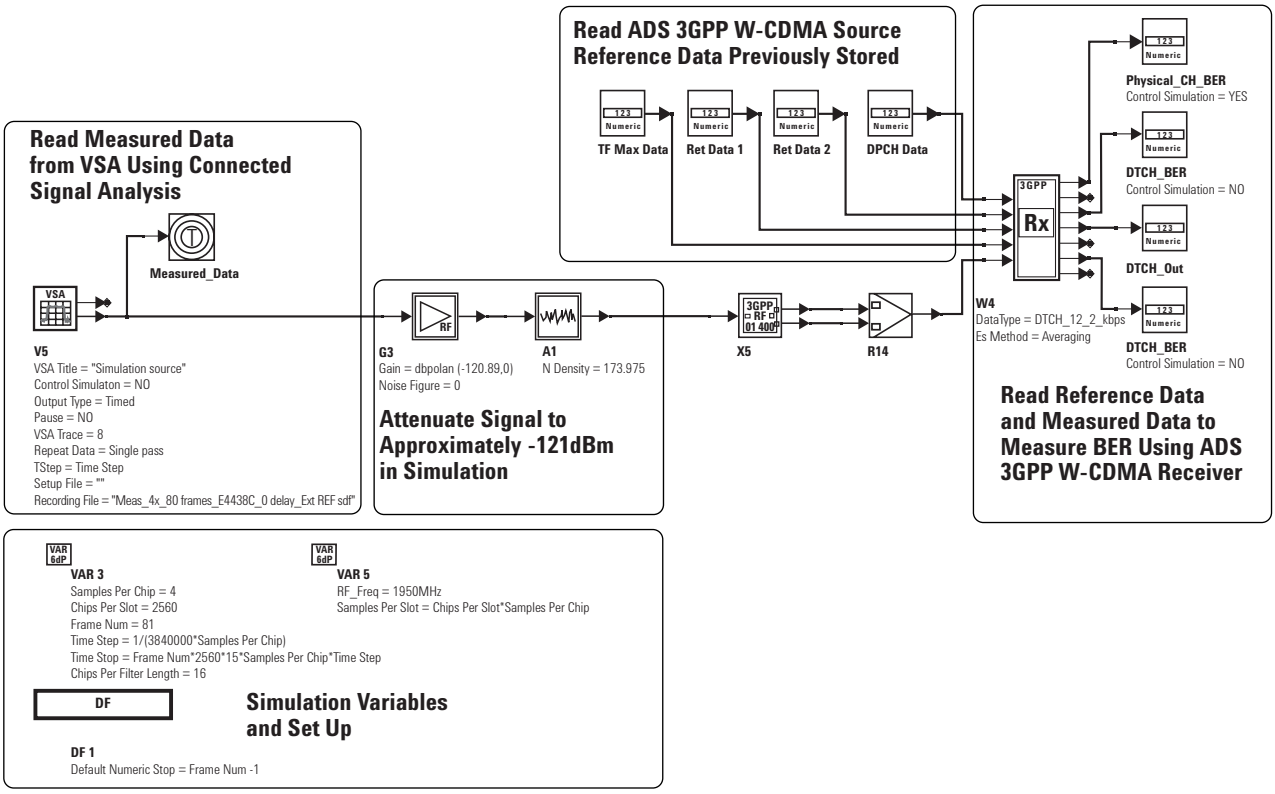


Figure 30. ADS Schematic to Read Recorded Measured Data and Measure BER

The 89600 source element is set up to read the previously recorded measured data file, as shown in figure 31. The measured signal is then attenated in simulation by passing it through a gain element in ADS with a negative gain. An AddNDensity element is cascaded behind the negative gain element to preserve the thermal noise floor in simulation. TkPower elements can be used to measure the total signal power at each stage.

Note that the signal power behind the AddNDensity will be dominated by the simulated thermal noise (-173.975 dBm +10 x log[3.84 MHz x 4] dB) in the simulation bandwidth.

The BER measurement simulation is set up for 80 frames. This can be changed to 3-4 frames initially to visually align and compare the simulated and measured waveforms, if desired.

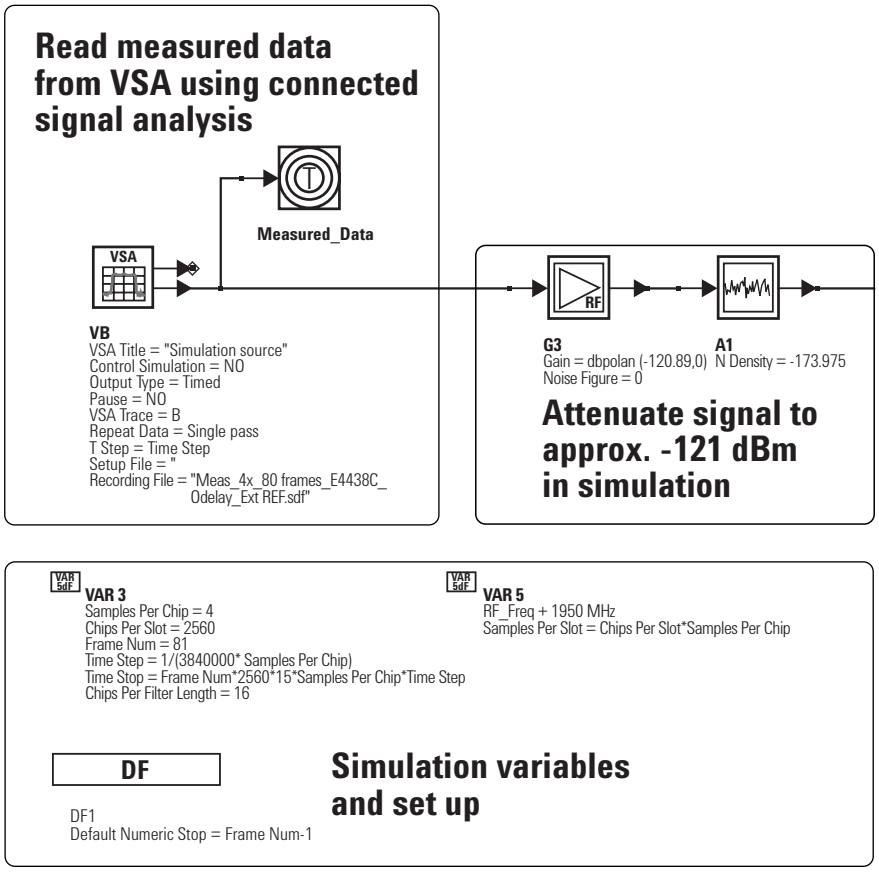


Figure 31. Close-up of 89600 Software Simulation Source configured to read measured data.

Note: The ADS W-CDMA receiver has a parameter named "EstMethod," which by default is set to "NoEst" for no channel estimation. Because there are physical delays associated with the measured signal, this parameter was changed to "Interpolation" so that the ADS W-CDMA receiver could accomodate delays associated with the measured signal.

Step 6. The BER simulation is run for a limited number of frames. An initial comparison of the reference and measured waveform shows a time offset, so a delay element is added to delay the reference waveform so that the measured and reference waveforms and demodulated bits can be overlaid on top of each other, as shown in at the top of figure 32.

The figure shows that the original simulated waveform agrees well with the recorded measured waveform being read back into simulation. It also shows that the original simulation data bits agree well with the data bits recovered from the recorded measured data.

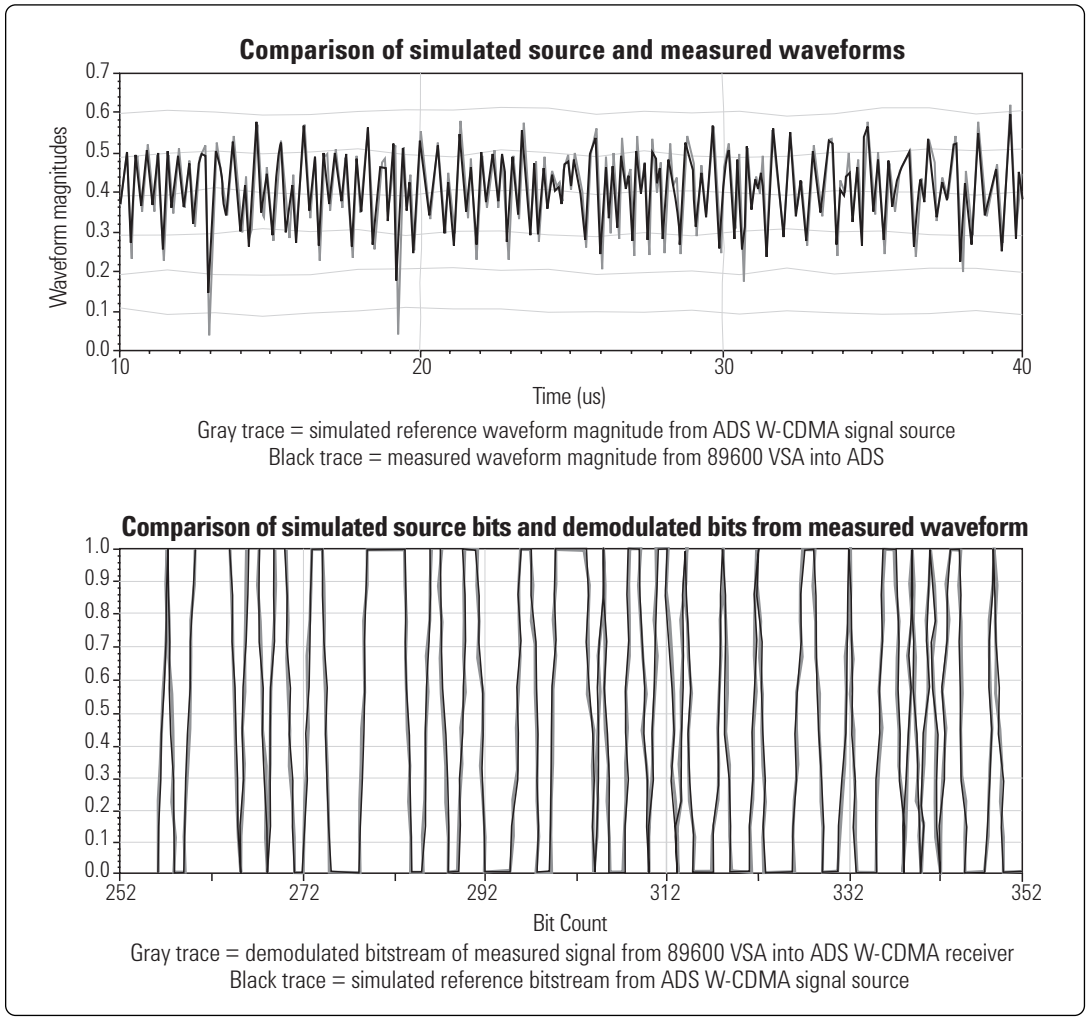


Figure 32. Reference and measured waveform overlaid on top of one another at top of figure. Reference bits and recovered measured bits overlaid on top of one another at bottom of figure.

Step 7. The simulation length is set back to 80 frames and the BER simulation is run. The results are shown in Figure 33, with the uncoded physical channel BER results shown at the top and coded BER results shown on the bottom.

The results shown in Figure 33 show a connected solutions coded BER result of 0 %, indicating that the data is properly synchronized. Note that the physical BER shown at the top of Figure 33 is non-zero. This is expected, since the physical BER does not include the benefits of coding gain.

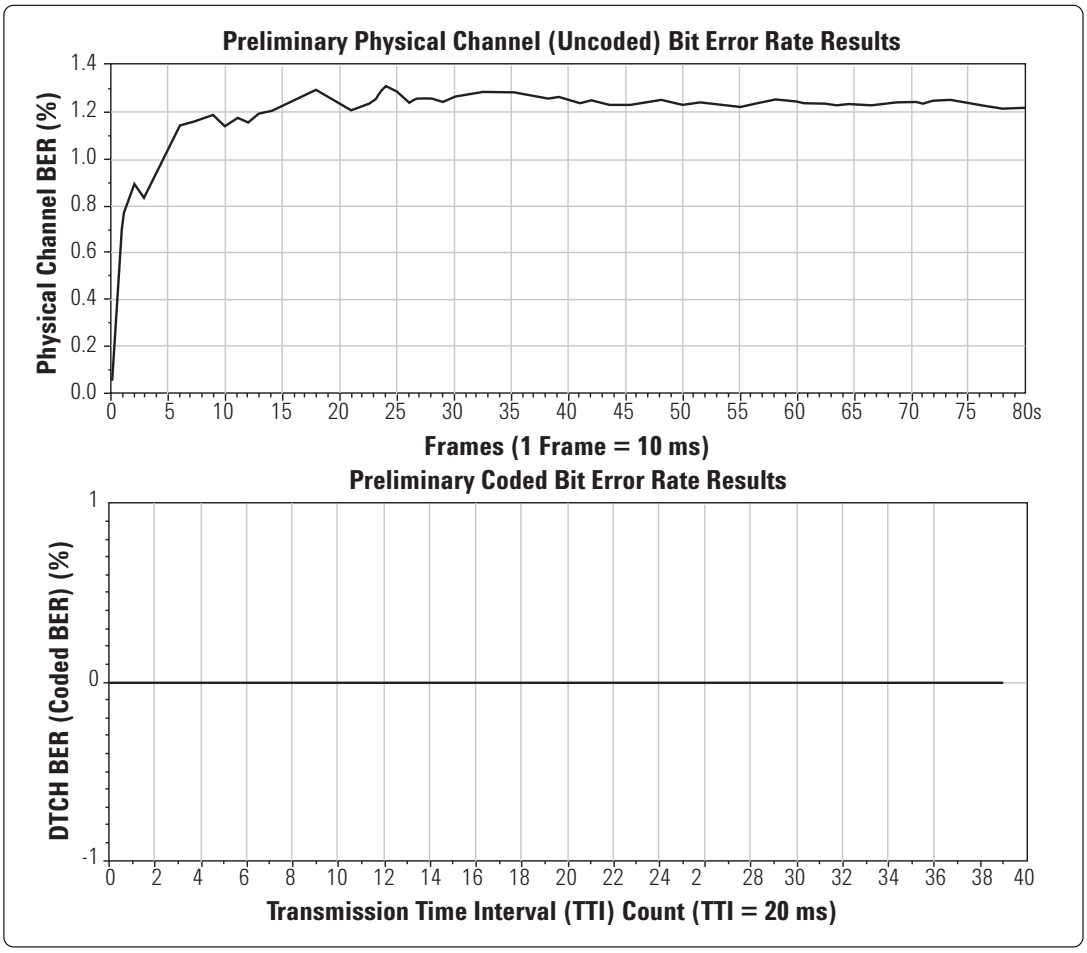


Figure 33. Connected solution uncoded BER result. The physical (uncoded) BER result is shown at top of figure. The coded BER result is shown at bottom of figure.

Step 8. Compare Connected Solution BER with Simulation BER. The schematic shown in Figure 34 is simulated to compute the physical and coded BER for simulation-only data. This will allow the connected solutions BER results to be compared with simulation-only BER results.

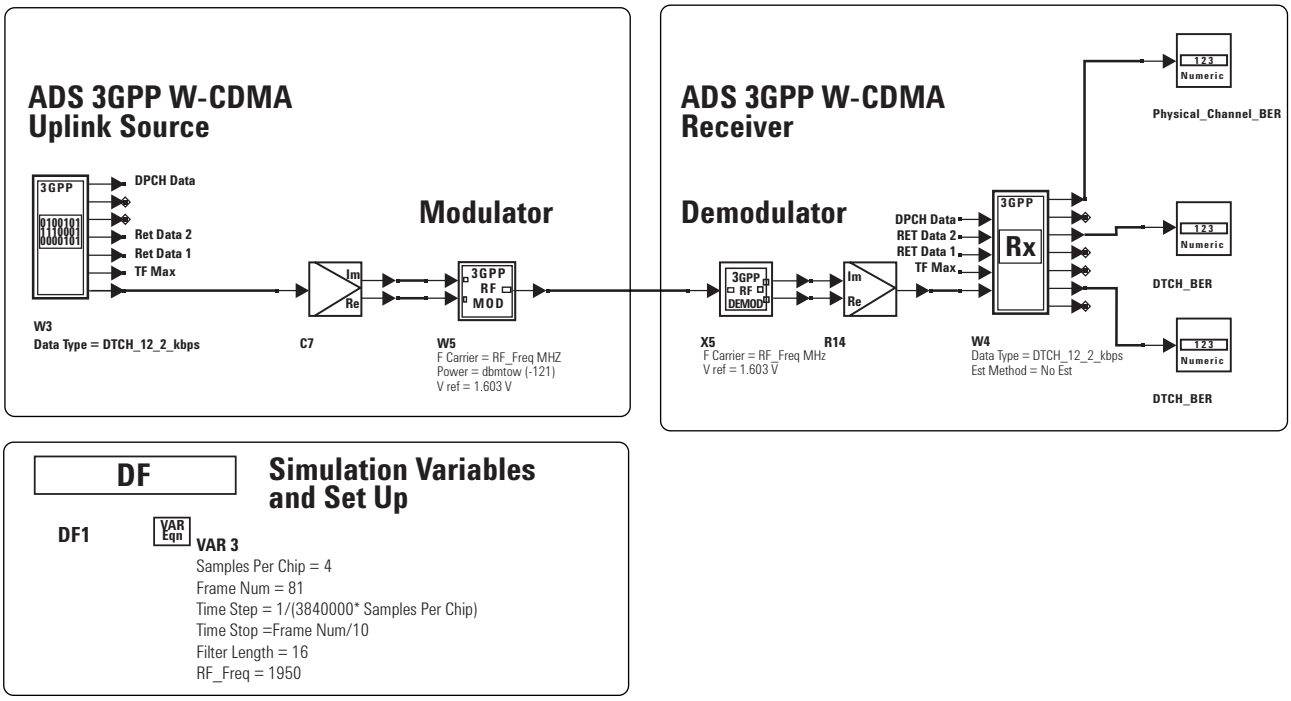


Figure 34. ADS Schematic to Simulate BER (no measured data).

Figure 35 shows a comparison of the connected solutions BER results and the simulation-only BER results.

The figure shows that the connected solutions BER results compare well with the simulation-only BER results. Both cases produce a 0% coded BER result, while the connected solution physical (uncoded) BER result (top black trace) is slightly degraded relative to the simulation-only physical BER result (top gray trace).

In summary, a connected solutions BER measurement shows good consistency with simulation-only BER results. Potential applications of this include:

- Measuring key components and determining their effect on BER by modeling the rest of the design in simulation
- Early BER verification of RF hardware, before the baseband hardware is completed (modeling the baseband functionality in ADS for coded BER)
- Early baseband BER verification by measuring the RF impairments and determining how well a baseband design modeled in simulation performs

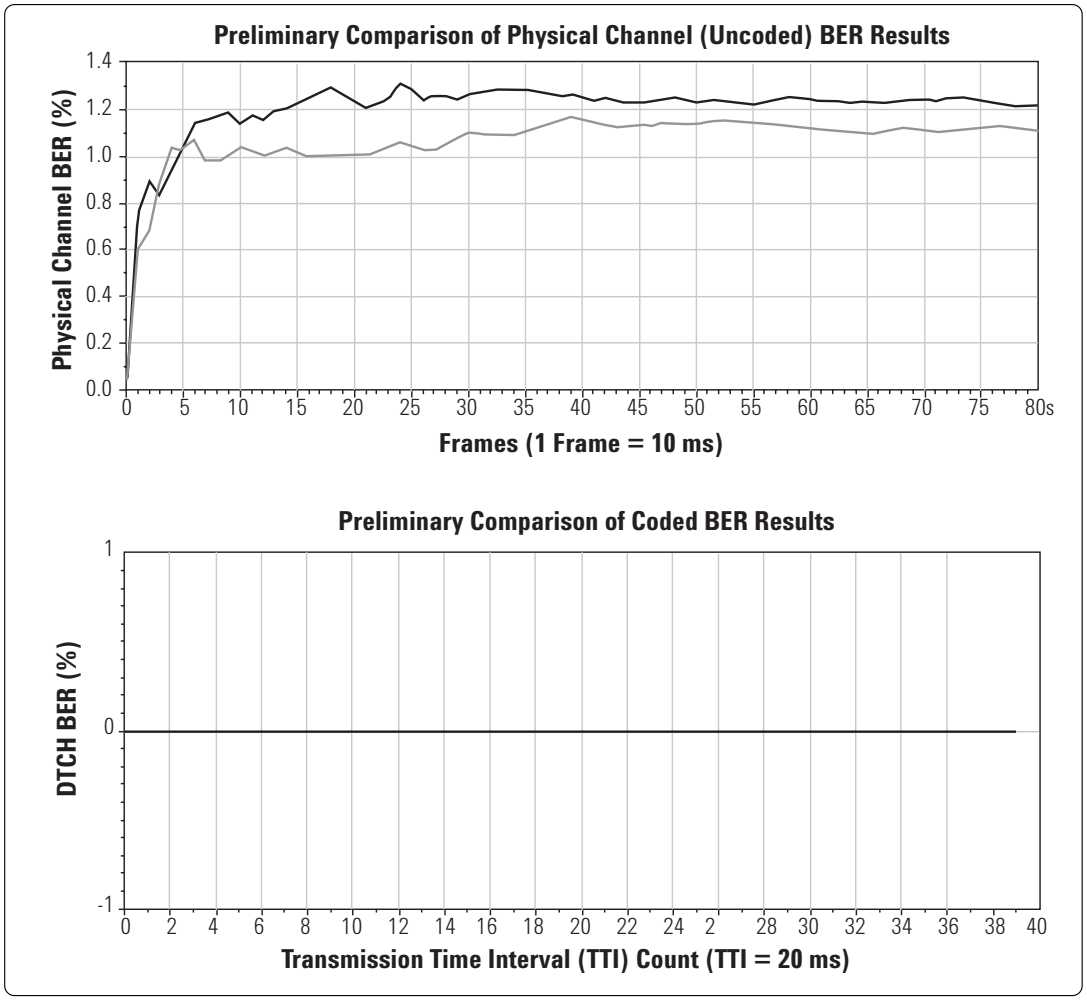


Figure 35. Comparison of connected solutions BER results and simulation-only BER results.

Appendix A: EDGE Connected Solution Examples

This appendix demonstrates how to configure the ADS-ESG sink and 89600 VSA for an EDGE signal format configuration.

The schematic in figure A1 was created by copying ADS2001\examples\ EDGE\EDGE_PA_Test_prj to a local subdirectory. The design EDGE_PA _MS_EVM.dsn contained within the copied project was then copied and edited as shown in the figure.

Notice that the **Instrument_Link _Variables** block contains a parameter **"Delay"** with a value of **20**. This was the delay observed from the signal source's linearized Gaussian filter by connecting a numeric sink (under Sinks\NumericSink in library) to the output of the ADS signal source.

The simulation is performed. Once the I and Q waveforms have been downloaded into the ESG arb, the ADS-defined signal can be activated by pressing the following keys on the ESG front panel:

Local > Mode > Arb Waveform Generator > Dual Arb > Select Waveform > "ADS_EDGE_SIGNAL"

Press the **Mod On/Off** and **RF On/Off** on the ESG front panel to turn on the RF output signal.

The ADS-defined EDGE signal is measured using an Agilent E4440 PSA. The test setup and corresponding baseline results are shown in figure A2. The measured rms average EVM is approximately 0.18%, because this is an ideal baseline case without impairments.

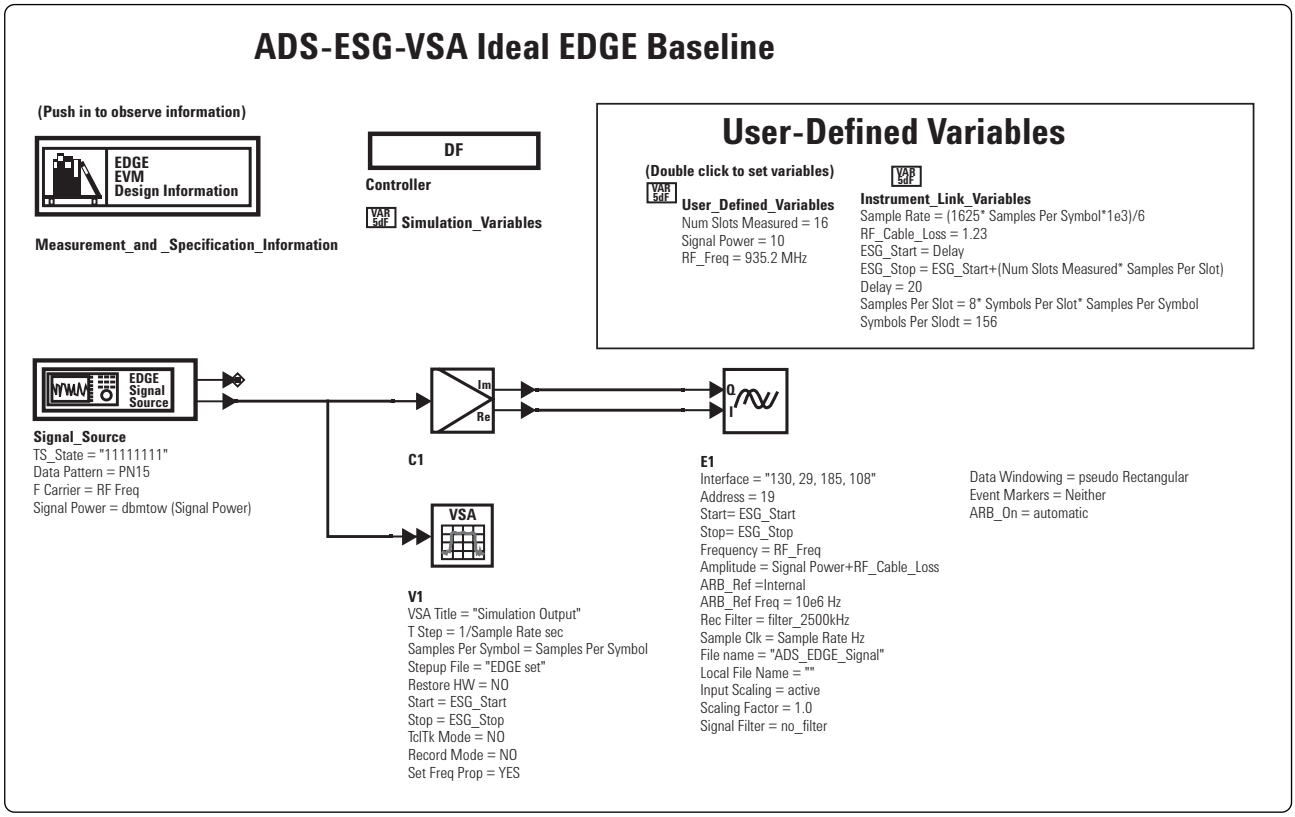


Figure A1. ADS schematic showing ADS-ESG ideal baseline configuration.

Note: "ADS_EDGE_SIGNAL" is the name specifiedas the "FileName" parameter on the ADS-ESG Sink.

The ADS schematic also contains an 89600 VSA measurement element. The ideal baseline simulation result with the 89600 VSA measurement element is shown below in figure A3. The rms EVM result is approximately 0.17%.

A setup file is stored and is referenced by the 89600 VSA. This display can also be configured by selecting the following on the 89600 VSA pull-down menu.

MeasSetup> Demodulator > Digital Demod
MeasSetup> Demod Properties...>Preset to Standard...> Cellular> EDGE

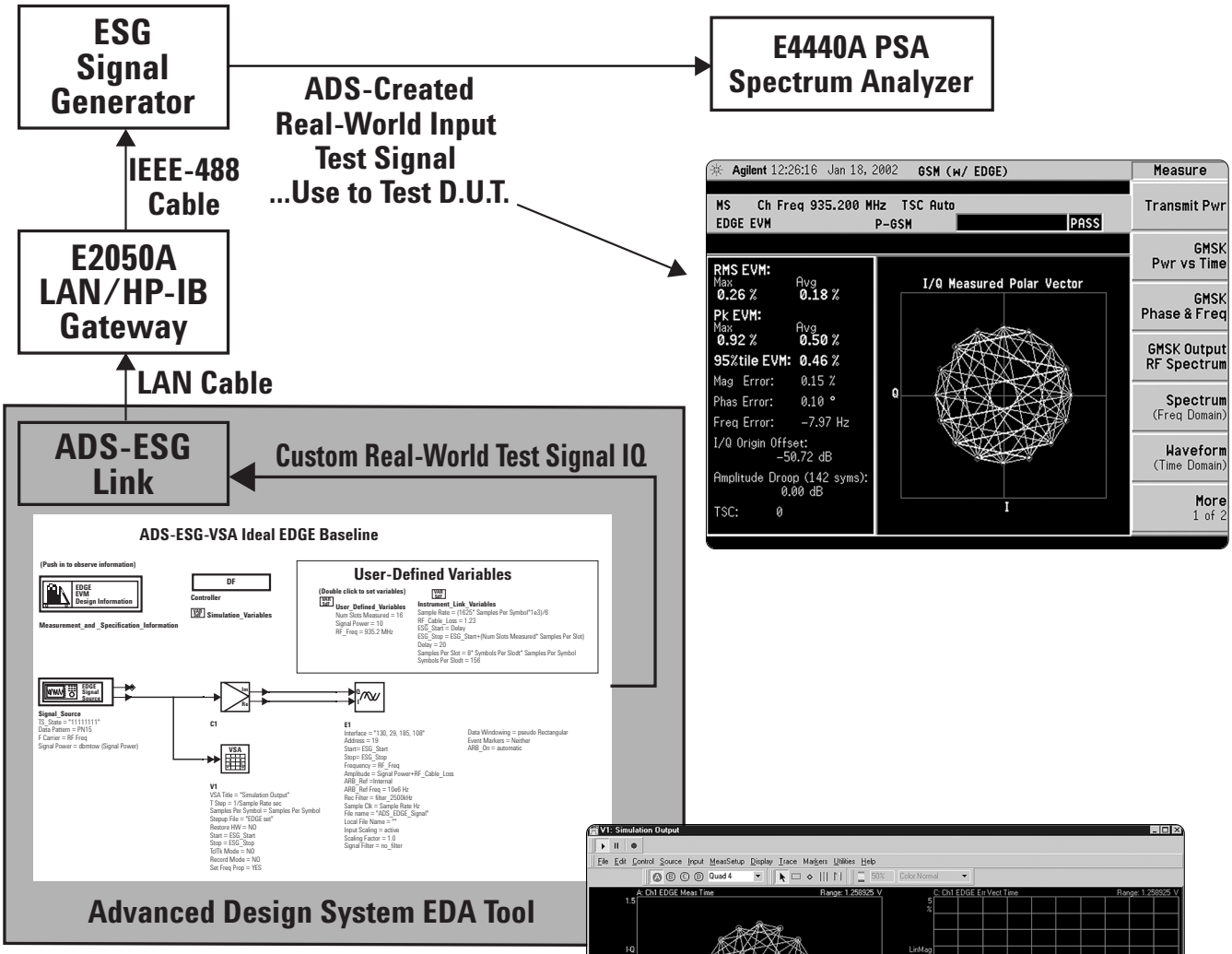


Figure A2. EDGE Baseline Case: Test setup measured results using the E4440 PSA showing 0.18 % EVM.

Figure A3. 89600 VSA results from ADS simulation.

We now extend this example to include amplitude and phase distortion introduced by modeling a driver amplifier and narrow-band filter in simulation, to evaluate a driver amplifier's performance with a real-world test signal input. The driver amplifier and bandpass filter are being modeled in simulation (for example, modeling hardware not available for test) to create a real-world test signal on the test-bench which contains impairments from the driver amplifier and filter. Modeling these impairments in simulation can allow verification testing of the power amplifier to begin at an earlier stage (for example, before the driver amplifier and filter hardware are available for testing) by creating this real-world test signal using the ADS-ESG sink.

The schematic shown in figure A4 is modified to include a driver amplifier and a 5th order bandpass Chebyshev filter with a 600 kHz 1dB bandwidth. The SignalPower parameter has been changed to 0 dBm so that the ADS EDGE signal source will output –15 dBm. The resulting schematic is shown in figure A4.

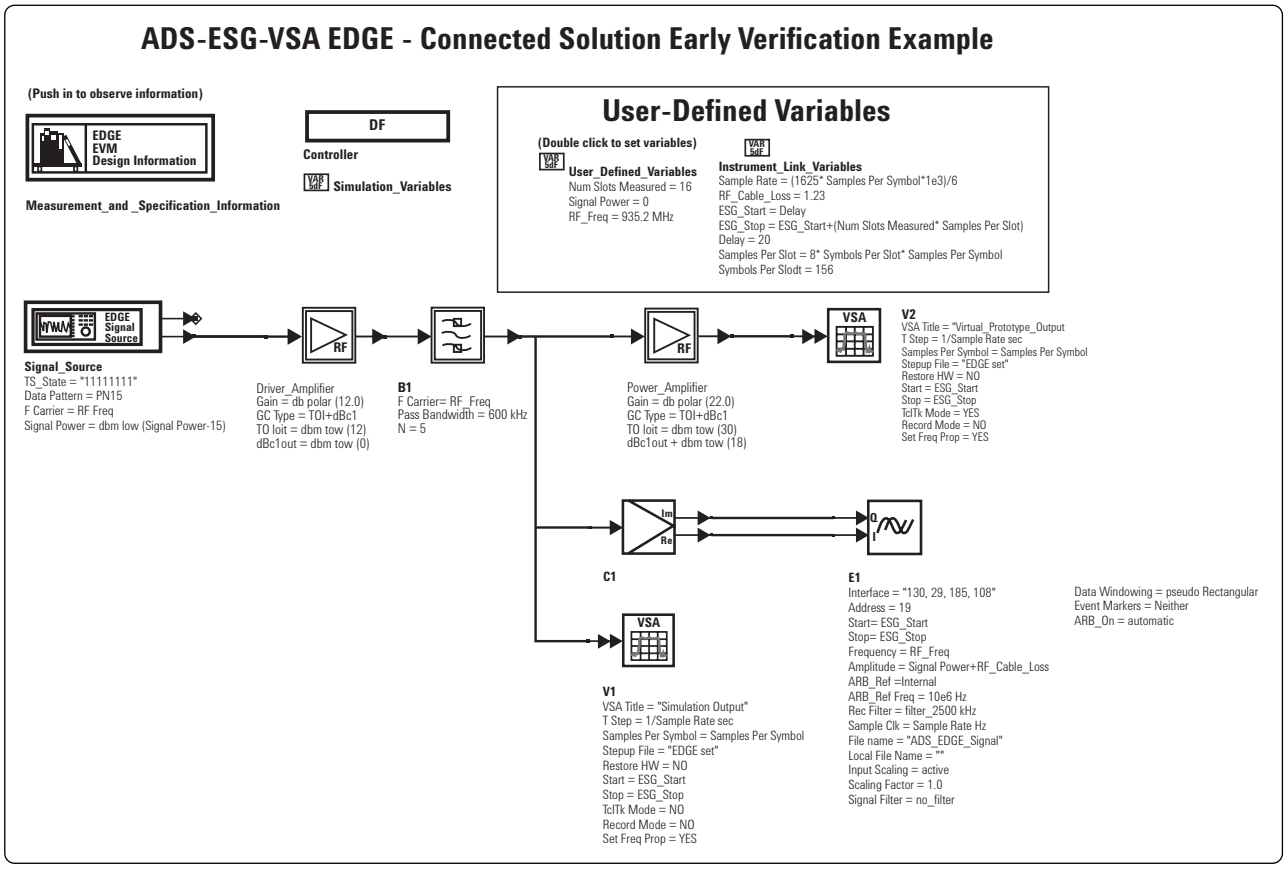


Figure A4. Early verification example with connected ADS-ESG solution.

The simulation is performed and the real-world output signal from the ESG is observed using the E4440A PSA as shown in figure A5. Note that the measured rms average EVM has degraded to 3.94% relative to the ideal baseline case first shown, reflecting the impairments modeled in simulation using ADS.

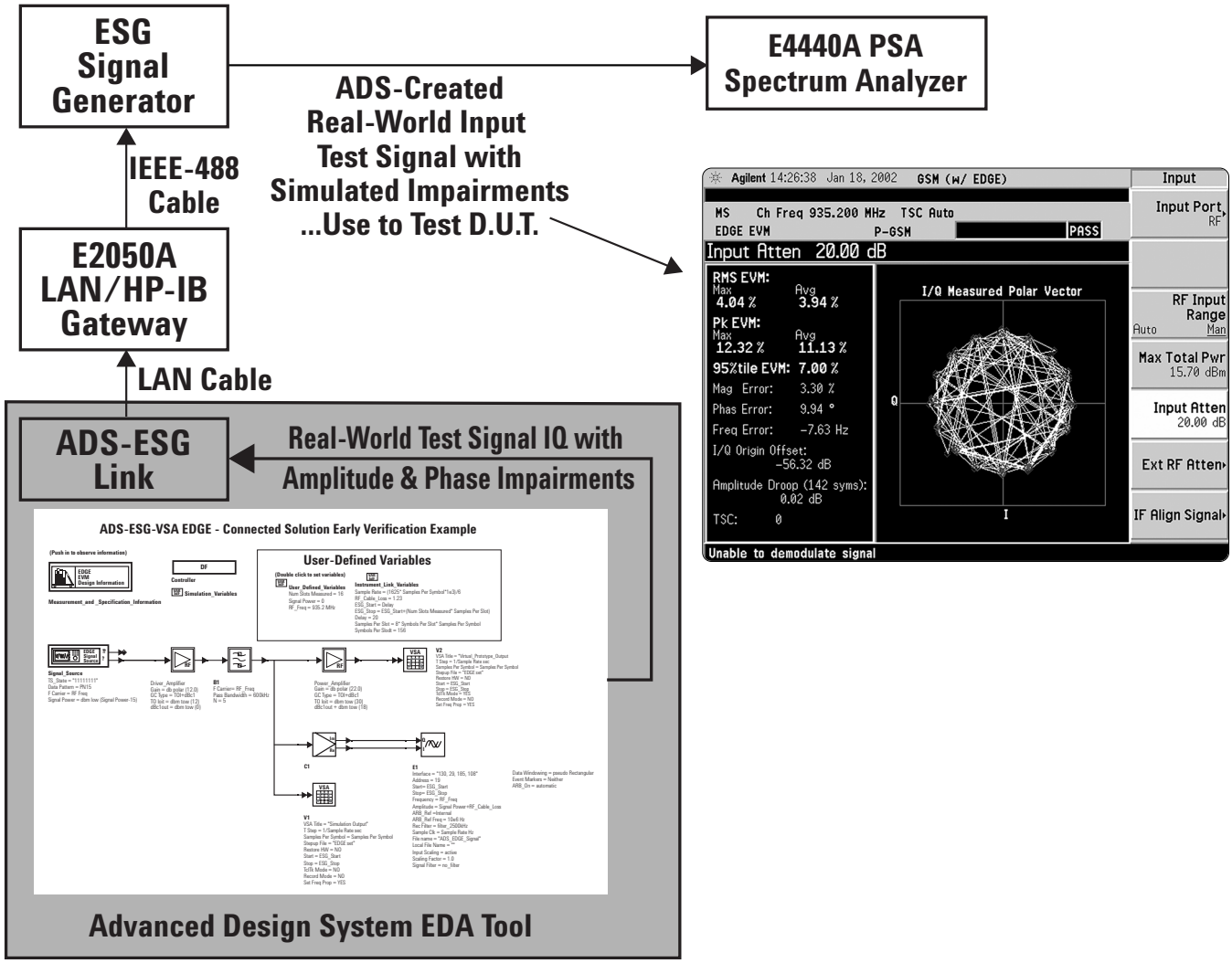


Figure A5. EDGE gain and phase distortion test case. Measured results using E4440 PSA showing degraded 3.94% EVM.

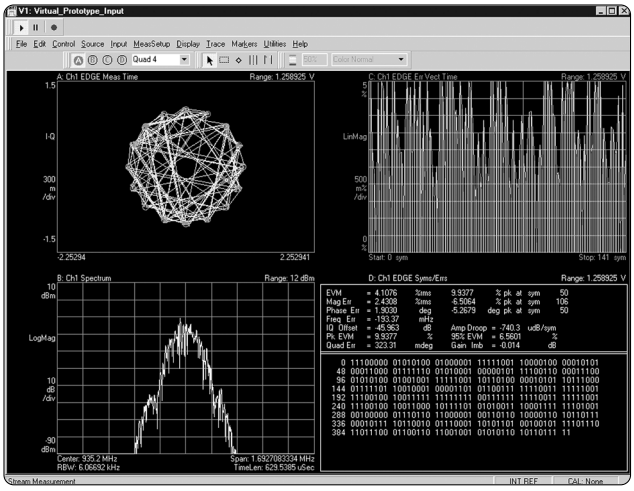
Figure A6 shows the corresponding simulation results using the 89600 VSA. Note that the simulated EVM has degraded to 4.1% (versus 3.94% measured), as a result of the amplitude, phase distortion, and inter-symbol-interference (ISI) introduced by the driver amplifier and bandpass filter. The simulated EVM of the power amplifier output using the 89600 VSA is 6.66%, which reflects the additional signal distortion introduced by the power amplifier.

Summary

The first example reflected a baseline configuration setup when using the ADS-ESG connected solution for EDGE. The ADS-ESG sink parameter settings shown can be used as a reference when using the ADS-ESG connected solution for EDGE applications.

The second example illustrates the early verification concept, combining simulation and test capability to facilitate early verification testing of prototype hardware.Hardware not yet available for testing can be modeled in simulation to create a custom, real-world test signal using the ADS-ESG connected solution. The 89600 VSA, which is dynamically linked in ADS, can be used to measure the modulated performance of simulated designs with a similar VSA user-interface and measurement algorithms available on the testbench.

"Real-World" Test Signal Input to PA



Simulated PA Output

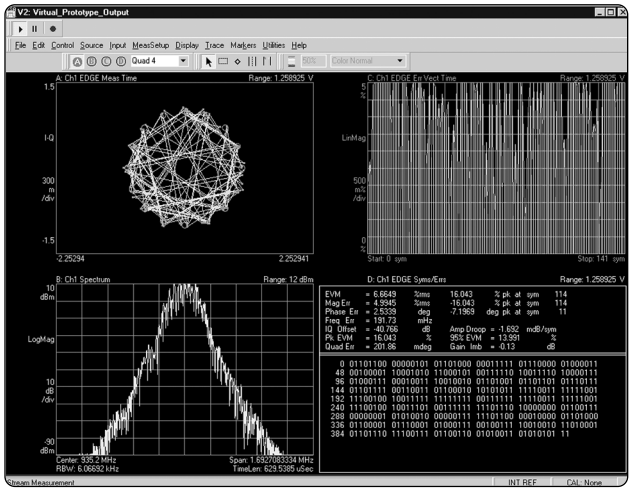


Figure A6. 89600 VSA results from ADS simulation with real-world input test signal shown on left and simulated output shown on right; Simulated EVM at input of PA is 4.1%; Simulated EVM at output of PA is 6.6%.

Appendix B: 1xEV-DO Connected Solutions Examples

This appendix demonstrates how to configure the ADS-ESG sink and 89600 VSA for a 1xEV-DO (Data Only) signal format configuration.

The schematic in figure B1 was created by copying ADS2001\ examples\1xEV\1xEV_PA_Test_prj to a local subdirectory. The design DSN_1xEV_FwdRho.dsn contained within the copied project was then copied and edited as shown in the figure. A phase equalizer was added to the ADS 1xEV-DO source for enhanced performance. Please contact Agilent EEsof EDA Technical Support at 1-800-473-3763 for details on how to download the latest project with the phase equalizer included.

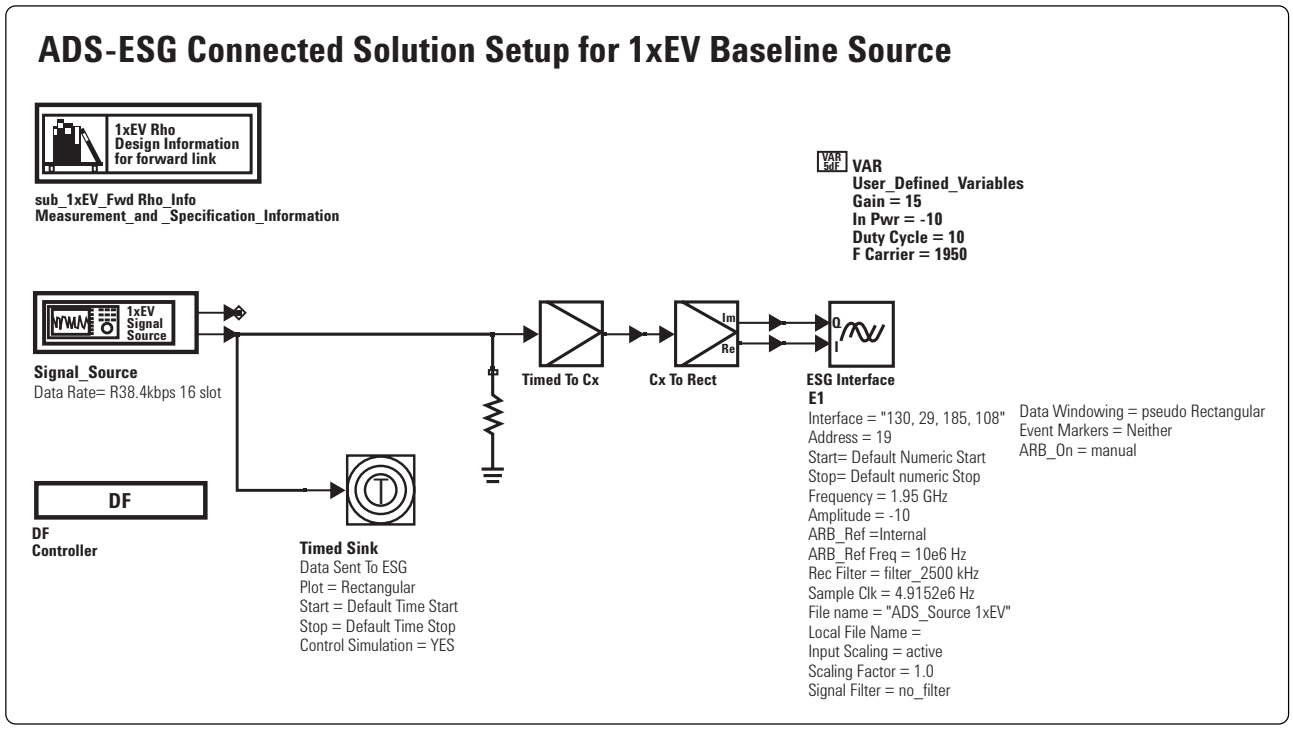


Figure B1. ADS schematic showing ADS-ESG 1xEV-DO ideal baseline configuration.

Note: "ADS_Source1xEV" is the name specified as the "FileName" parameter on the ADS-ESG sink.

The simulation is performed. Once the I and Q waveforms have been downloaded into the ESG arb, the ADS-defined signal is activated by pressing the following keys on the ESG front panel:

Local > Mode > Arb Waveform Generator > Dual Arb > Select Waveform> "ADS_Source1xEV"

The **Mod On/Off** and **RF On/Off** on the ESG front panel can then be pressed to turn on the RF output signal.

The ADS-defined 1xEV-DO signal is measured using an Agilent E4440 PSA. The test setup and corresponding baseline results are shown in figure B2. The measured rho is .99976 rms and the average EVM is approximately 1.57%, since this is an ideal baseline case without impairments.

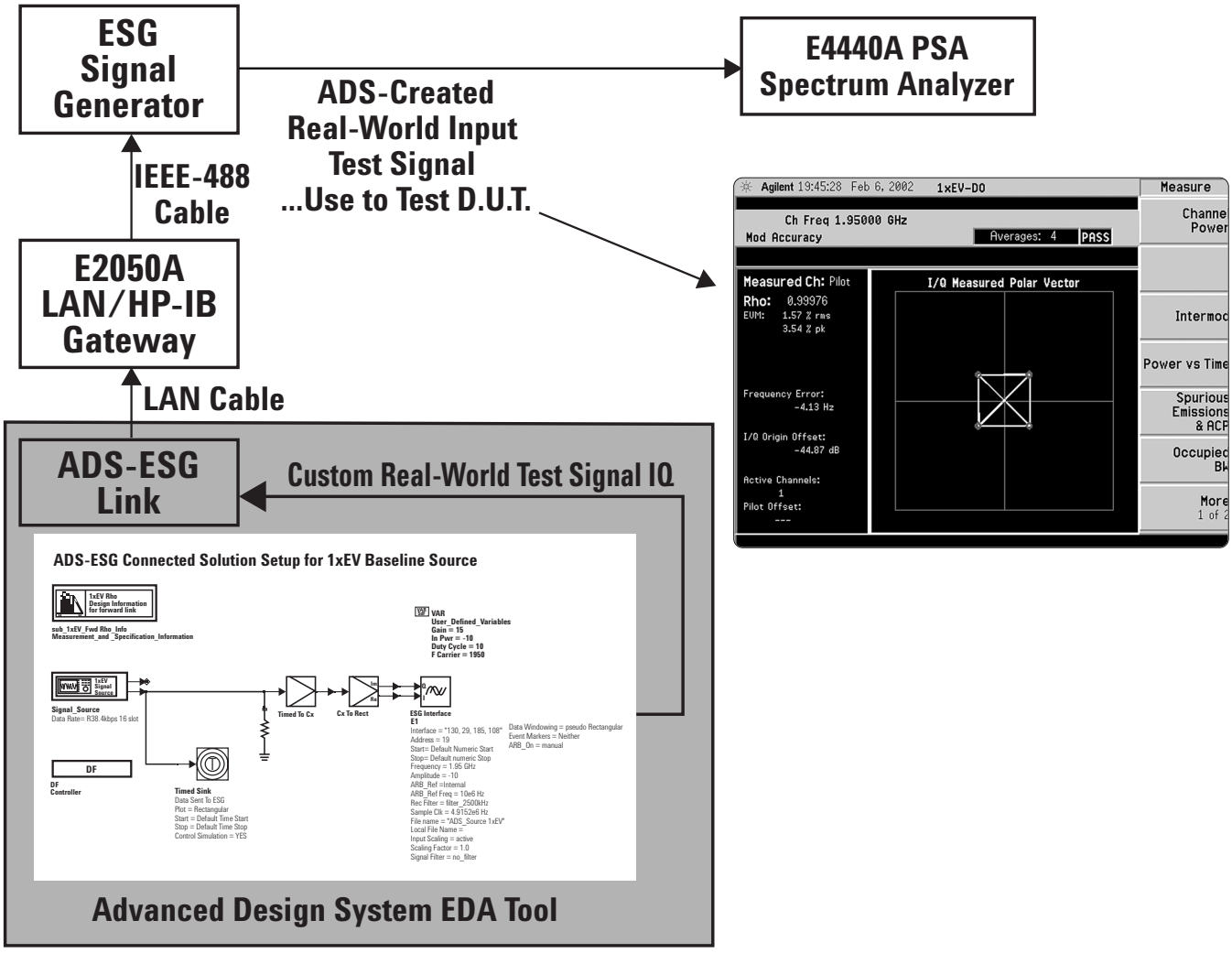


Figure B2. 1xEV-DO Baseline Case: Test setup and ideal baseline measured results using the E4440 PSA.

We extend this example to include amplitude and phase distortion introduced by modeling a driver amplifier and narrowband filter in simulation, to evaluate a driver amplifier's performance with a real-world test signal input. The driver amplifier and bandpass filter are being modeled as "simulation prototypes" (for example, test hardware not available) to create a custom real-world test signal on the testbench which contains impairments from the driver amplifier and filter. Modeling these impairments in simulation can allow verification testing of the power amplifier to begin at an earlier stage (for example, before the driver amplifier and filter hardware are available for testing) by creating this custom real-world test signal using the ADS-ESG sink.

The schematic is modified to include a driver amplifier and a 5th order bandpass Chebyshev filter with a 5.5-MHz, 1-dB bandwidth. The Power parameter has been changed to -13 dBm on the ADS 1xEV-DO signal source. The resulting schematic is show in figure B3.

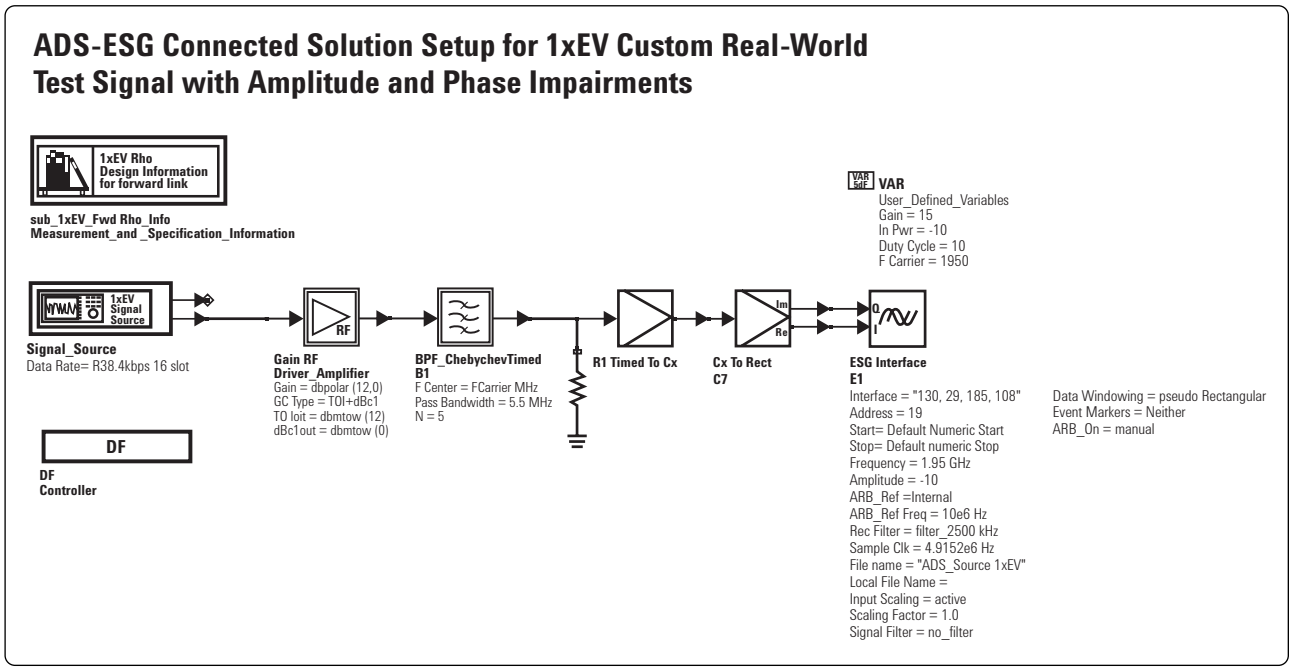


Figure B3. 1xEV gain and phase distortion case with ADS-ESG connected solutions.

The simulation is performed and the custom real-world output signal from the ESG is observed using the E4440A PSA as shown in figure B4. Note that the rho has degraded to 0.99735 and measured rms average EVM has degraded to 5.17% relative to the ideal baseline case first shown, reflecting the impairments modeled in simulation using ADS.

Summary

The first example shows a baseline configuration setup when using the ADS-ESG connected solution for 1xEV-DO. The ADS-ESG sink parameter settings shown could be used as a reference when using ADS-ESG sink connected solutions for 1xEV-DO.

The second example illustrates the early verification concept, combining simulation and test capability to facilitate early verification testing of prototype hardware. Hardware not yet available for testing can be modeled in simulation to create a custom real-world test signal using the ADS-ESG connected solution.

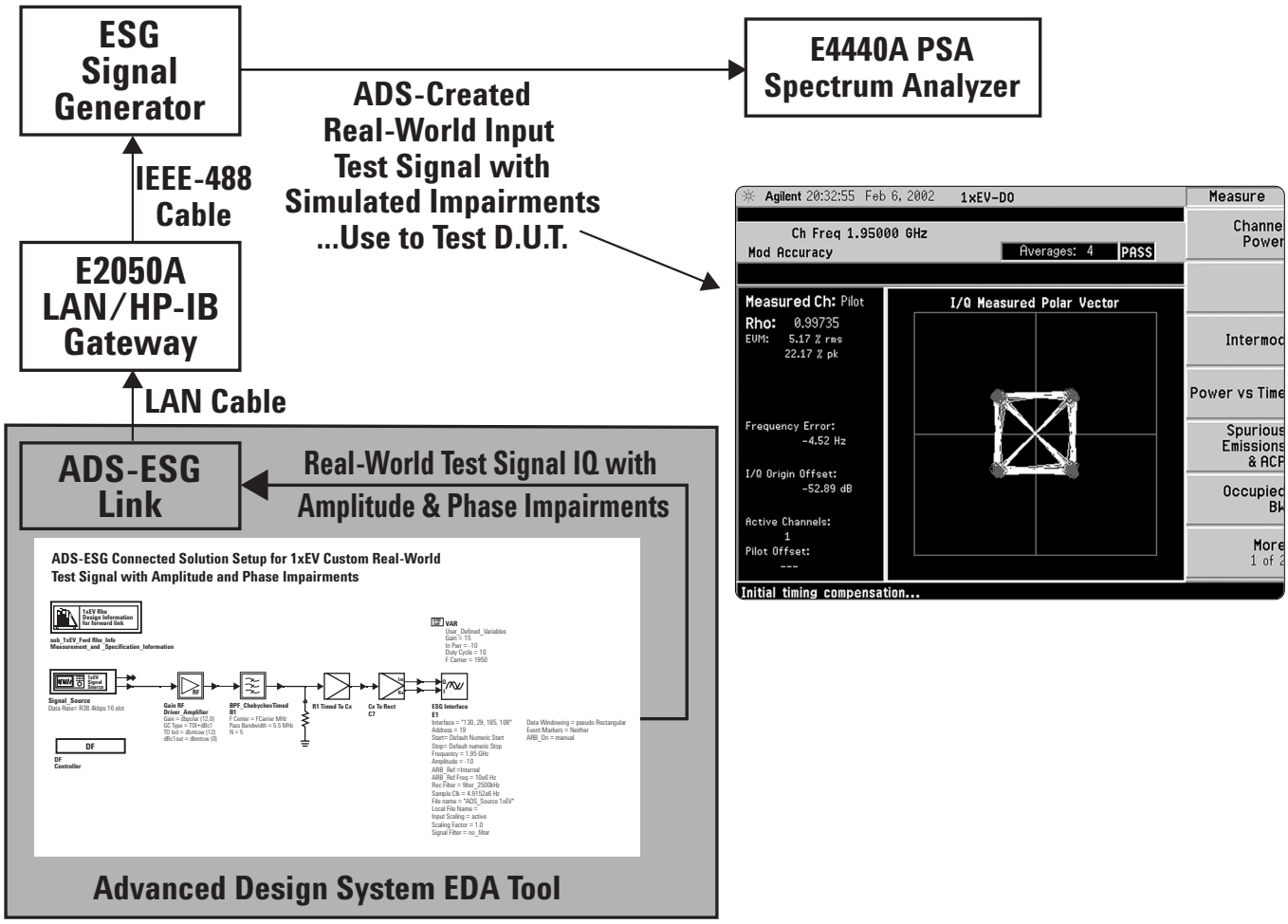


Figure B4. 1xEV-DO gain and phase distortion test case: Setup and measured results using E4440 PSA, showing degraded 5.17% EVM relative to baseline case.

Appendix C: WLAN 802.11a Example

This appendix demonstrates how to configure the ADS-4438C ESG Sink for WLAN 802.11a. The schematic in Figure C1 was created by copying ADS\examples\WLAN\WLAN_PA_80211a_Test_prj project to a local subdirectory. The design WLAN_PA_80211a_EVM.dsn contained within the copied project was then copied and edited as shown in figure C1, using the ESG4438CSink:

The ADS simulation source is configured for a 54 Mb/s data rate with a 5.8 GHz center frequency. The ESG4438CSink is configured with the parameter settings shown for optimal performance using the ESG4438CSink. The baseline test setup is shown in figure C2.

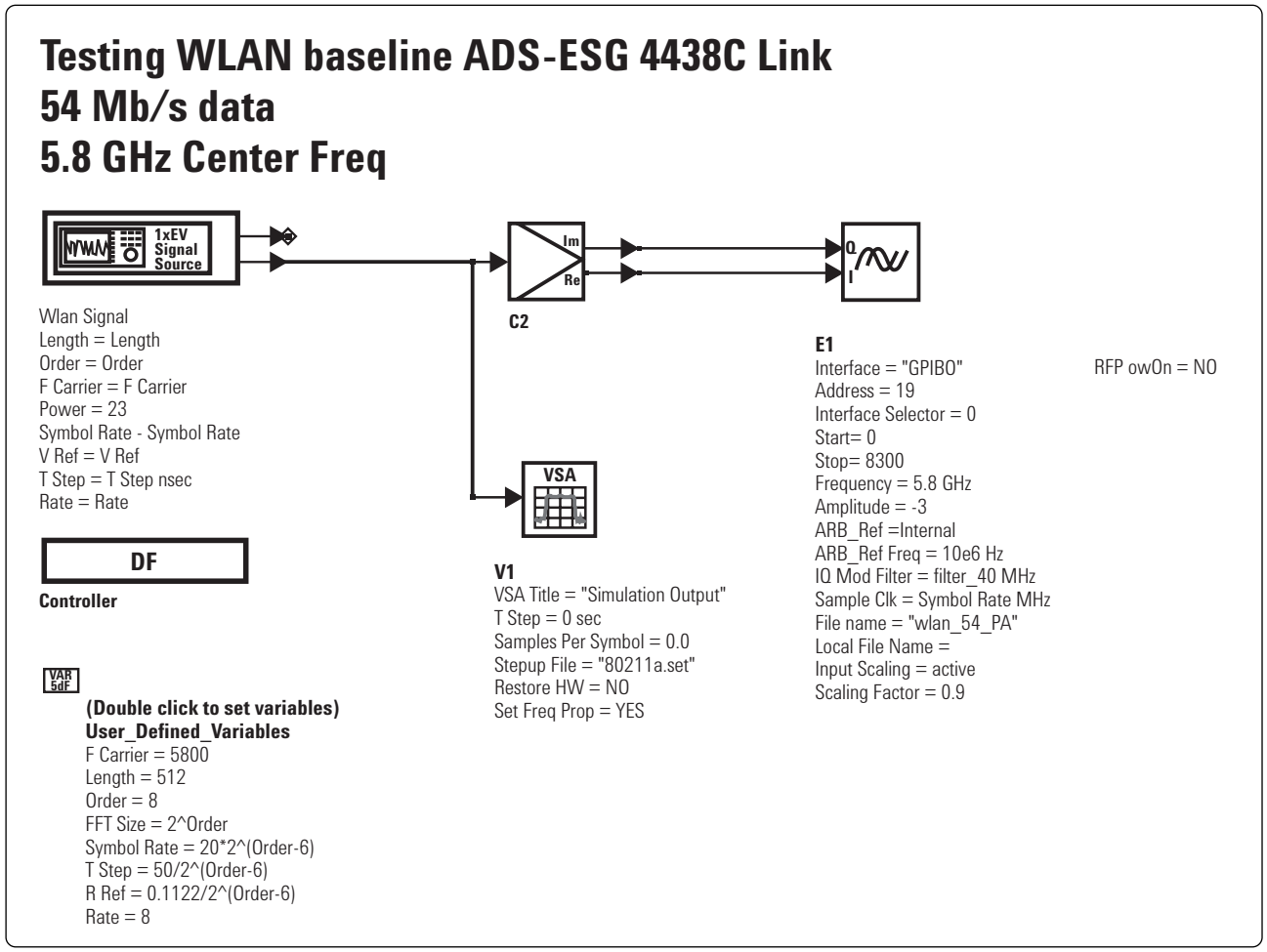


Figure C1. Baseline ADS-ESG4438CSink setup.

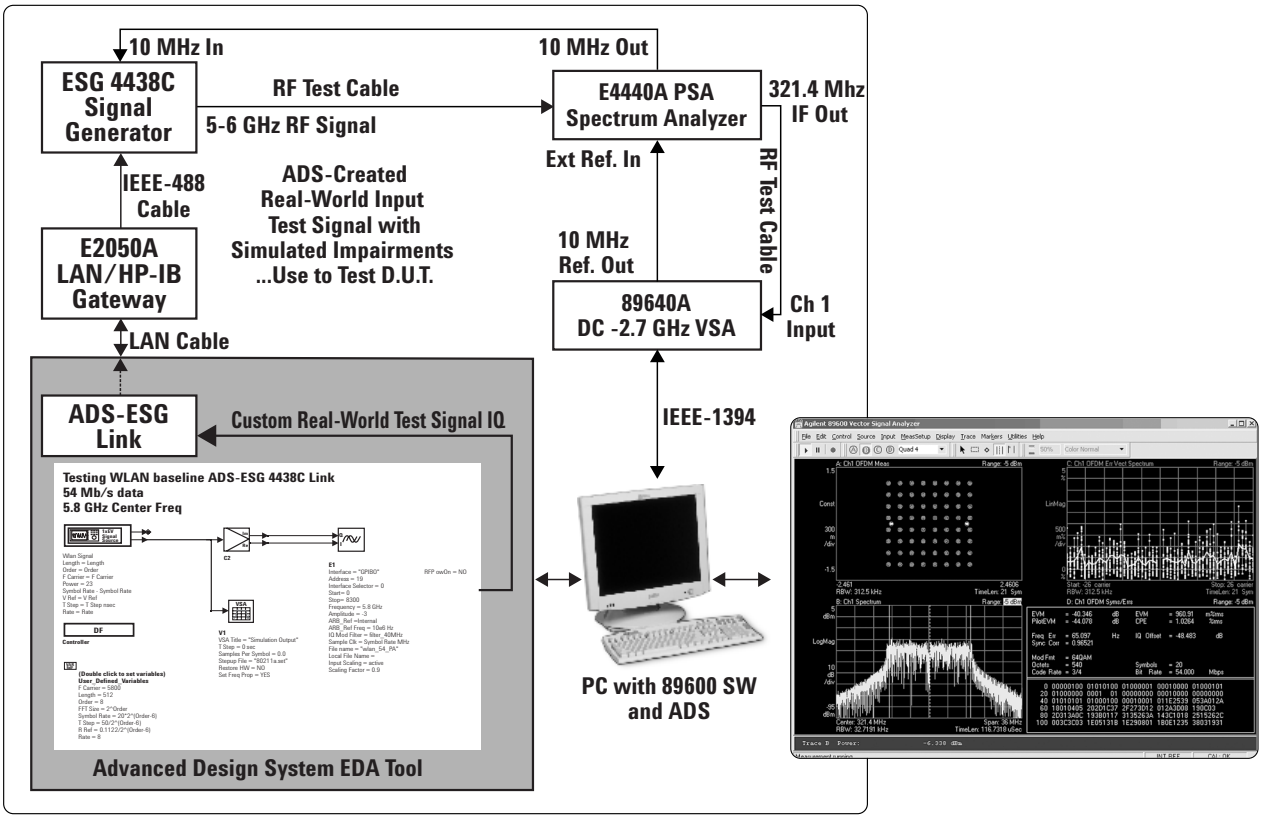


Figure C2. ADS, E4438C ESG, E4440A PSA, and 89640 VSA baseline test setup for WLAN 802.11a.

The ADS-defined signal using the ADS-ESG4438C Sink is demodulated using the 89640 VSA and measured results are shown in figure C3, with a residual EVM of approximately 0.96% showing good baseline performance. Simulated results are shown in figure C4.

In summary, this appendix shows a setup using the ADS-ESG4438CSink, E4438C ESG signal generator, E4440A PSA, and 89640 VSA for a WLAN 802.11a connected solution baseline example. This preliminary example could be useful as a starting point for other WLAN connected solution applications, such as modeling RF and other impairments in ADS and creating a real-world test signal on the testbench for early verification testing.

For other examples from the Agilent wireless networking seminar, visit: **http://contact.tm.agilent.com/tmo/eesof/news/wireless_networking.html**

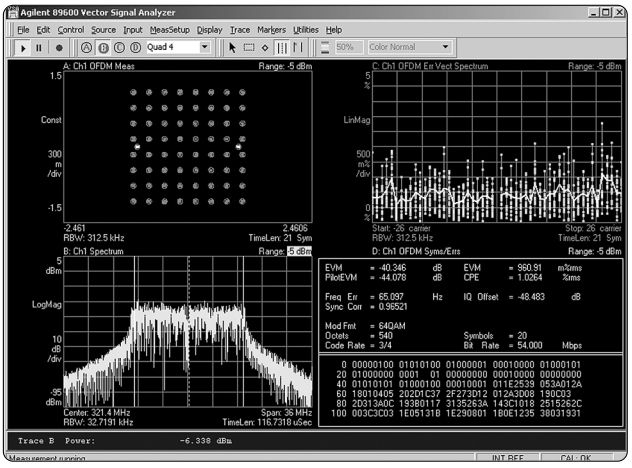


Figure C3. Measured results on the 89640 VSA using the ADS-ESG4438C Sink.

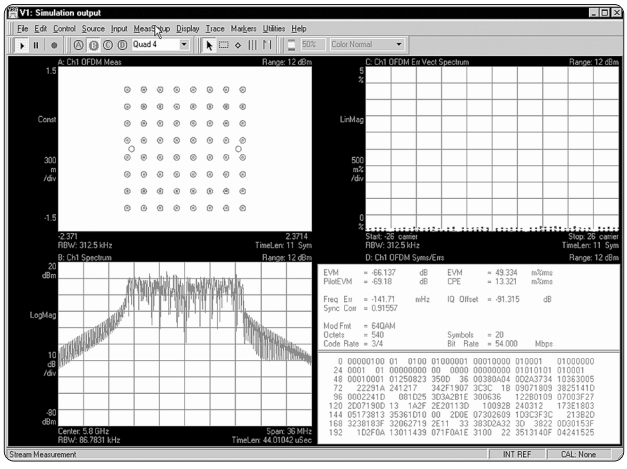


Figure C4. Simulated results using the 89600 VSA software in ADS.

Appendix D: Configuring the ADS-E443XB ESG Sink

This appendix discusses configuring the existing ADS-ESG sink for E443XB ESG signal generators.

ADS can communicate with the ESG signal generator either through a GPIB card or a LAN/GPIB gateway. The GPIB option requires a GPIB card to be used with the PC or UNIX platform on which ADS is installed.

If “lan” is instead typed in for the Interface parameter, then a LAN/GPIB Gateway can instead be used to communicate with the instrument. Using a LAN/IP Gateway allows the instrument to be accessed through an IP address on a network. This allows PC/UNIX platform with ADS to be physically distant from the ESG test equipment if network connections allow it.

The supported configurations for GPIB interface cards and LAN/GPIB are shown in Table D1 for various operating systems supported by ADS.

Configuring the ADS-ESG Sink for a GPIB Card

Install the software that came with the GPIB interface card, and set the Interface parameter to the card's symbolic name: typically, HPIB for Agilent cards and GPIB for National Instruments cards, possibly followed by a number. Set the “Address” parameter on the ADS-ESG Sink to the instrument GPIB address.

Operating System	Agilent interface cards	National instruments interface cards	Agilent E2050A LAN/GPIB
HP-UX 10.2x/HP-UX 11	Agilent E207x	GPIB-HP700-EISA	yes
SunOS 5.6, 5.7, and 5.8		PCI-GPIB (PCI), GPIB-SPRC-B (SBus)	yes
Windows 95, 98, 2000, NT 4.0	Agilent 8234x, 8235x	PCI-GPIB, PCMCIA-GPIB, AT-GPIB	yes
IBM AIX 4.3 or higher			yes

Table D1. Supported Interface Card and LAN/GPIB Gateway Configurations.

Configuring the ADS-ESG Sink for a LAN/GPIB Gateway

For Windows and HP-UX 10.2x, download the drivers from **http://www.agilent.com/find/iolib**

ADS provides appropriately configured drivers for all other platforms.

- For Windows, follow the install instructions on the web page. Run the IO Config program at *Start:Programs:HP I_O Libraries:I_O Config*. From the *Available Interface Types* on the left column, click on **Lan Client > Configure > ok**. The default settings are correct.
- For HP-UX 10.2x, follow the install instructions on the web page. As root, run */opt/sicl/bin/iosetup*. Run the IO Config program at *Start:Programs:HP I_O Libraries:I_O Config*. From the *Available Interface Types* on the left column, click on **Lan Client > Configure > ok**. The default settings are correct.
- Set the Interface parameter to the E2050A IP address or host name. The instrument model assumes the LAN interface is LAN and the E2050A interface is HPIB; if not, use the explicit LAN[192.168.0.1]: HPIB, substituting the LAN interface for LAN, the E2050A interface for HPIB, and the IP address inside the square braces. Set the “Address” parameter on the ADS-ESG interface to the instrument's GPIB address.

Appendix E: Configuring the ADS-E4438C ESG Sink

This appendix discusses configuring the ADS-E4438C ESG Sink for E4438C ESG signal generators.

Setting up IO for the ESG4438C Sink

Since the ESG4438C Sink link uses the Agilent IO Libraries VISA layer for communication over GPIB and/or LAN interfaces, it is necessary for a user to configure a VISA Interface.[1] The most recent version of Agilent IO libraries can be downloaded from this IO Libraries website. Download the K.01.00 self-installing I/O Libraries file iolibs.exe (6.5 Mb). Then execute it to install the I/O Libraries. The version of the IO library supported is K.01.00.00 or later. This documentation is not meant to be a guide to setup IO interfaces. For comprehensive information, refer to the IO Libraries Installation and Configuration Guide for Windows and VISA User's Manual.

Select an installation that includes SICL and VISA IO libraries. To configure interfaces for use with the ESG4438CSink, run the IO configuration application by right clicking the IO icon in the icon tray and selecting Run IO Config.

IO Config Utility

The IO Config Utility can be used to configure instruments over several different interfaces. The IO Config application is shown in figure E1.

Adding a VISA Interface

Among the interfaces available, those pertinent to ESGs in general are the following:

TCPIP Interface

To use instruments across a LAN or using a HPIB/LAN box, a TCPIP interface needs to be added.

Choose VISA Type: TCPIP [Interface Description: LAN Client (LAN Instruments)] and click Configure. Accept the default values provided and click OK.

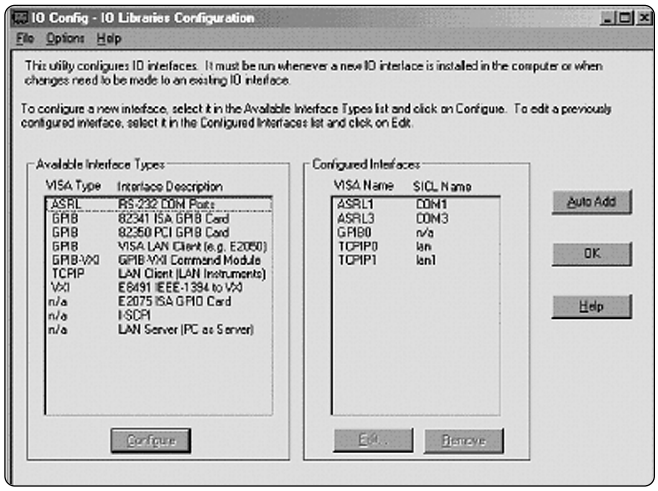


Figure E1. IO Config Utility.

A new VISA interface named TCPIP<x> is added to the list, where x is a number. This number is assigned to the InterfaceSelector parameter of the ESG4438CSink model. After the interface has been added, it is necessary to configure it before it can be used.

GPIB Interface

- Local GPIB interface

  This means a GPIB card is available in the local PC on which ADS is installed. To configure the interface for this card, choose the appropriate option based on the *Interface Description* provided. Click OK. If a valid GPIB interface is found a new interface is added to the IO configuration
- Remote GPIB Interface

  A remote GPIB interface could be an E2050 HPIB/LAN box or a PC that has a local GPIB interface configured and has a LAN server running.

  To configure an E2050, a TCPIP Interface has to be configured first.

  Choose VISA type: GPIB [Interface Description: VISA LAN Client (for example, E2050)] and click configure.

  Set
  Remote Hostname to <hostname> or <ipaddress> of the LAN box.
  Remote SICL Interface Name to the <hpib_name> (for example, hpib)

  Set
  Remote Hostname to <hostname> or <ipaddress> of the LAN box.
  Remote SICL Interface Name to the <hpib_name> (for example, hpib)

  Click OK. A new VISA interface is added to the list of interfaces. It is necessary to *configure* this interface before it can be used.

1 The ESG Interface component used the SICL library and therefore did not need the additional VISA configuration step mentioned above.

Configuring a VISA Interface
Configuring a TCPIP Interface

To configure the TCPIP<x> interface, select it and click Edit->Edit Visa Configuration.
Click Add Device and enter the machine name or IP address, and the device name or bus address.
Click Ok on all the boxes to save the configuration.

Configuring a GPIB Interface

After either one of these two types of GPIB interfaces have been added to the list of configured interfaces, a VISA name is assigned to the GPIB<x> interface, where x is a number. This number is assigned to the Interface-Selector parameter of the ESG4438C Sink model. Choose the interface that needs to be configured and click Edit->Edit Visa Configuration. Instruments can be added manually, or click Auto Add Devices. If there are any instruments connected via GPIB cables to the local/remote GPIB interface, they will show up on the device list, which looks like this.

Click OK in all the boxes to save the configuration.

To use a configured GPIB<x> interface, set the following parameters of the ESG4438CSink model.

Interface =	GPIB
Address =	<bus address of instrument for example, 19>
InterfaceSelector =	<x e.g 0>

Appendix F: Troubleshooting ADS-ESG Sink Issues

Symptom – ESG returns “out of memory” error message.

Troubleshooting Tips:

1. Check the number of samples to be downloaded into ESG Arb with ADS-ESG sink. The Stop-Start parameter should not exceed the maximum number of samples supported by the E443XB or E4438C ESG signal generator being used.
2. Save any desired arb waveforms into non-volatile memory by pressing Mode> Arb Waveform Generator > Dual Arb> Waveform Segments > Store Segment to NVARB Memory.
3. Cycle power on ESG to clear any existing Arb waveform in memory.
4. Re-simulate.

Symptom – Signal bandwidth looks incorrect when viewing ADS-ESG signal with Spectrum Analyzer, VSA, or PSA.

Troubleshooting Tips:

1. Check that the SampleClk parameter on the ADS-ESG sink has the same sampling rate as the signal in the ADS simulation (for example, 1/TimeStep).
2. Check that the SampleClk parameter on the ADS-ESG sink has the correct frequency units (for example, MHz).
3. Check that the RecFilter parameter on the ADS-ESG sink has a greater bandwidth than the simulated signal bandwidth.

Symptom – ACPR/ACLR results look better than simulated ACPR/ACLR, especially at large frequency offsets.

Troubleshooting Tips:

1. Check that the RecFilter parameter on the ADS-ESG sink has a greater bandwidth than (frequency offset + measurement bandwidth/2). It may need to be set to “through” setting when performing ACPR/ACLR with large frequency offsets.
2. Check that the SignalFilter parameter is set to “no_filter”, if there is already a transmit baseband filter in the ADS modulator.

Note: To check to see if a newly added interface has been configured correctly, try using the VISA Assistant utility.
Note: If for some reason, an error message pops up when Auto Add Devices is selected, there is probably an error in the configuration. The VISA Assistant utility can be used to troubleshoot the configuration. For more information read the VISA documentation.

Appendix G: Troubleshooting ADS- 89600 VSA Interface Issues

Symptom – 89600A Signal Source does not produce a stimulus signal in ADS.

Troubleshooting Tips:

1. Exit ADS.
2. Ensure that LAN cable or GPIB cable is connected to VSA/PSA; Power down and power up PSA if LAN connection was not properly connected.
3. If using LAN connection, then ping the IP address of the VSA/PSA to verify connection.
4. Bring up Taskmanager (for example, ctrl-alt-delete on Windows NT). Click on "Applications" tab and End any leftover "AgtVsaVector" processes. Click on "Processes" tab and End any leftover "VSAVEC.EXE" processes.
5. Run IO Config. Ensure that GPIB0 appears as a configured interface.
6. Double-click on GPIB0. Ensure that the hostname correctly reflects the IP address, if using a LAN connection:
7. Run VISA Assistant. Ensure that GPIB0 reflects the GPIB address of the VSA/PSA.
8. Click on the "Formatted I/O" tab of VISA Assistant. Click on "SCPI" in lower-right corner and then "*IDN?" button. Verify that VSA/PSA is appears and that the firmware version (for example, A.02.04) is supported by the 89600 VSA.
9. Start the 89600 VSA by selecting "Start> Programs > Agilent 89600 VSA> Vector Signal Analyzer". Verify that the 89600 now identifies the connected hardware.

Appendix H: Additional Information

Product Information:
ADS Products and Wireless Design Libraries:
http://contact.tm.agilent.com/tmo/eesof/products/

Agilent Solution Brochures:
Wireless 2G/3G Solutions:
www.agilent.com/find/3G

Solutions for Designing and Manufacturing Base Transceiver Stations and Their Components:
www.agilent.com/find/basestationtest

Solutions for Designing and Manufacturing Wireless Appliances:
www.agilent.com/find/wirelessdesign

Application Notes:
ADS Application Information/Papers/Application Notes:
http://contact.tm.agilent.com/tmo/eesof/applications/

3G Application Notes:
www.agilent.com/find/3G

Configuration Guides:
EDA-Instrument Connected Solutions
Publication Number 5988-6561EN

ADS Wireless Networking Seminar Papers and ADS Projects:
http://contact.tm.agilent.com/tmo/eesof/news/wireless_networking.html

Training Classes:
ADS Circuit/System; 3GPP W-CDMA; EDGE Design Classes:
http://contact.tm.agilent.com/tmo/eesof/education/

Appendix I: List of Accronyms and Abbreviations

3GPP – Third Generation Partnership Project
ACLR – Adjacent Channel Leakage Ratio
ADS – Advanced Design System
Arb – ESG Signal Generator Arbitrary Waveform Generator
BER – Bit Error Rate
CCDF – Complimentary Cumulative Distribution Function
DAC, D/A – Digital to Analog Converter
DSP – Digital Signal Processing
DUT – Device Under Test
ESG – E443XB ESG Signal Generator
EVM – Error Vector Magnitude
FIR – Finite Impulse Response
GPIB – General Purpose Interface Bus
HPIB – HP Interface Bus
IC – Integrated Circuit
IO – Input / Output
LAN/IP – Local Area Network / Internet Protocol
LO – Local Oscillator
OFDM – Orthogonal Frequency Division Multiplexing
PLL – Phase Locked Loop
PSA – E4440A Performance Signal Analyzer
RF – Radio Frequency
RRC – Root Raised Cosine
SW – Software
VISA – Virtual Instrument Software Architecture
VSA – Vector Signal Analyzer
WCDMA – Wideband Code Division Multiple Access
WLAN – Wireless Local Area Network

Agilent Technologies' Test and Measurement Support, Services, and Assistance
Agilent Technologies aims to maximize the value you receive, while minimizing your risk and problems. We strive to ensure that you get the test and measurement capabilities you paid for and obtain the support you need. Our extensive support resources and services can help you choose the right Agilent products for your applications and apply them successfully. Every instrument and system we sell has a global warranty. Support is available for at least five years beyond the production life of the product. Two concepts underlie Agilent's overall support policy: "Our Promise" and "Your Advantage."

Our Promise
Our Promise means your Agilent test and measurement equipment will meet its advertised performance and functionality. When you are choosing new equipment, we will help you with product information, including realistic performance specifications and practical recommendations from experienced test engineers. When you use Agilent equipment, we can verify that it works properly, help with product operation, and provide basic measurement assistance for the use of specified capabilities, at no extra cost upon request. Many self-help tools are available.

Your Advantage
Your Advantage means that Agilent offers a wide range of additional expert test and measurement services, which you can purchase according to your unique technical and business needs. Solve problems efficiently and gain a competitive edge by contracting with us for calibration, extra-cost upgrades, out-of-warranty repairs, and on-site education and training, as well as design, system integration, project management, and other professional engineering services. Experienced Agilent engineers and technicians worldwide can help you maximize your productivity, optimize the return on investment of your Agilent instruments and systems, and obtain dependable measurement accuracy for the life of those products.

Get the latest information on the products and applications you select.

By internet, phone, or fax, get assistance with all your test and measurement needs.

For more information about Agilent EEsof EDA visit: **www.agilent.com/find/eesof**

Online assistance:
www.agilent.com/find/assist

Phone or Fax
United States:
(tel) 800 452 4844

Canada:
(tel) 877 894 4414
(fax) 905 282 6495

China:
(tel) 800 810 0189
(fax) 800 820 2816

Europe:
(tel) (31 20) 547 2323
(fax) (31 20) 547 2390

Japan:
(tel) (81) 426 56 7832
(fax) (81) 426 56 7840

Korea:
(tel) (82 2) 2004 5004
(fax) (82 2) 2004 5115

Latin America:
(tel) (305) 269 7500
(fax) (305) 269 7599

Taiwan:
(tel) 0800 047 866
(fax) 0800 286 331

Other Asia Pacific Countries:
(tel) (65) 6375 8100
(fax) (65) 6836 0252
Email: tm_asia@agilent.com

Information subject to change without notice.

Printed in USA August 26, 2002
5988-6044EN

Agilent Technologies